SY89874U

2.5 GHz, Any Differential In-to-LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination

Features

- Integrated Programmable Clock Divider and 1:2 Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
  - >2.5 GHz f_{MAX}
  - <250 ps t_r/t_f
  - <15 ps Within-Device Skew
- Low Jitter Design:
  - <10 ps_{PP} Total Jitter
  - <1 ps_{RMS} Cycle-to-Cycle Jitter
- Unique Input Termination and V_T Pin for DC-Coupled and AC-Coupled Inputs; CML, PECL, LVDS, and HSTL
- TTL/CMOS Inputs for Select and Reset
- 100KEP-Compatible LVPECL Outputs
- Parallel Programming Capability
- Programmable Divider Ratios of 1, 2, 4, 8, and 16
- Low-Voltage Operation: 2.5V or 3.3V
- Output Disable Function
- –40°C to +85°C Temperature Range
- Available in 16-Pin (3 mm x 3 mm) QFN Package

Applications

- SONET/SDH Line Cards
- Transponders
- High-End Multiprocessor Sensors

United States Patent No. RE44,134

General Description

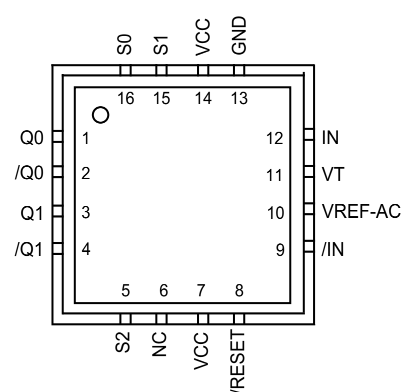
This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622 MHz or higher) CML, LVPECL, LVDS, or HSTL clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. Available divider ratios are 2, 4, 8, and 16, or straight pass-through. In a typical 622 MHz clock system this would provide availability of 311 MHz, 155 MHz, 77 MHz, or 38 MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

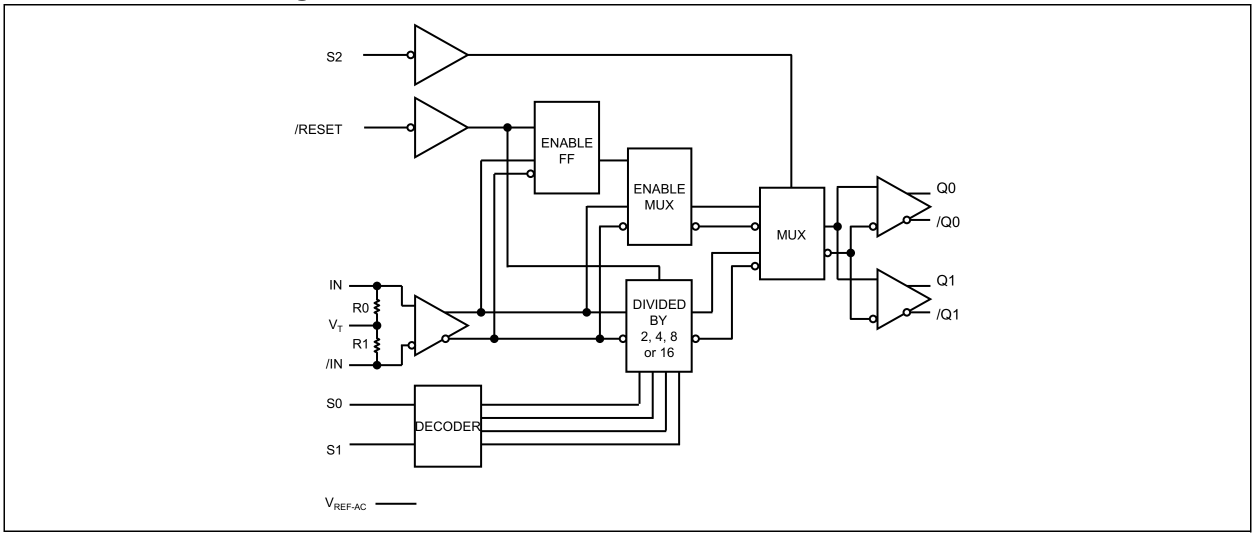
The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN).

Package Type

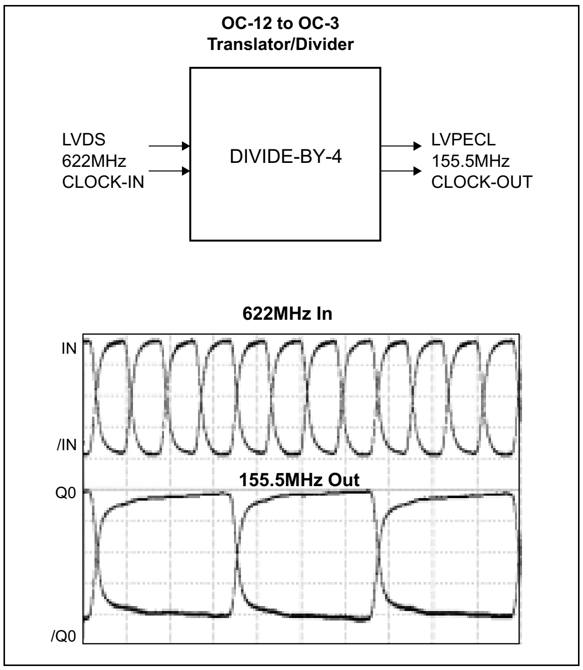
SY89874U
3 mm x 3 mm QFN-16 (M)
(Top View)



Functional Block Diagram



Typical Performance



TRUTH TABLE

/RESET	S2	S1	S0	Outputs
1	0	X	X	Reference clock (pass-through)
1	1	0	0	Reference clock ÷ 2
1	1	0	1	Reference clock ÷ 4
1	1	1	0	Reference clock ÷ 8
1	1	1	1	Reference clock ÷ 16
0	1	X	X	Q = Low, /Q = High clock disable

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC} + 0.3V
ECL Output Current
    Continuous .... 50 mA
    Surge .... 100 mA
Input Current IN, /IN (I_{IN}) .... ±50 mA
V_T Current (I_{VT}) .... ±100 mA
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$) (Note 1) .... ±2 mA

Operating Ratings ††

Supply Voltage (V_{CC}) .... +3.3V ±10% or +2.5V ±5%

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply	V_{CC}	2.375	—	3.63	V	—
Power Supply Current	I_{CC}	—	50	75	mA	No load, max. V_{CC}
Differential Input Resistance (IN-to-/IN)	R_{IN}	90	100	110	Ω	—
Input High Voltage (IN, /IN)	V_{IH}	0.1	—	V_{CC} + 0.3	V	Note 2
Input Low Voltage (IN, /IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	Note 2
Input Voltage Swing	V_{IN}	0.1	—	V_{CC}	V	Note 2, Note 3
Different Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 2, Note 3, Note 4
Input Current (IN, /IN)	I_{IN}	—	—	45	mA	Note 2
Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	Note 5

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Due to the internal termination (see Input Buffer Structure), the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit. Performance might be impacted if the differential inputs are driven single-ended.

3: See Timing Diagram for V_{IN} definition. V_{IN} (maximum) is specified when V_{IN} is floating.

4: See Definition of Single-Ended and Differential Swing section for V_{DIFF} definition.

5: Operating using V_{REF-AC} is limited to AC-coupled PECL or CML applications only. Connect directly to the V_T pin.

LVPECL (100KEP) DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} – 2V, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{CC} – 1.145	V_{CC} – 1.020	V_{CC} – 0.895	V	—
Output Low Voltage	V_{OL}	V_{CC} – 1.945	V_{CC} – 1.820	V_{CC} – 1.695	V	—
Output Voltage Swing	V_{OUT}	550	800	1050	mV	—
Differential Output Voltage Swing	V_{DIFF_OUT}	1.10	1.60	2.10	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the LVPECL (100KEP) Electrical Characteristics table after thermal equilibrium has been established.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	–125	—	20	µA	—
Input Low Current	I_{IL}	–300	—	—	µA	—

Note 1: The circuit is designed to meet the DC specifications shown in the LVTTL/CMOS Electrical Characteristics table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} – 2V, unless otherwise stated. Note 1, Note 2

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Output Toggle Frequency	f_{MAX}	2.5	—	—	GHz	Output swing ≥400 mV
Maximum Input Frequency		3.2	—	—		Divide by 2, 4, 8, 16
Differential Propagation Delay IN-to-Q	t_{PD}	540	650	790	ps	Input swing <400 mV
		480	600	730		Input swing ≥400 mV
Within Device Skew (Differential) Q0 - Q1	t_{SKEW}	—	7	15	ps	Note 3
Part-to-Part Skew (Differential)		—	—	250		
Reset Recovery Time	t_{RR}	600	—	—	ps	Note 4
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	1	ps_{RMS}	Note 5
Total Jitter		—	—	10	ps_{PP}	Note 6
Additive Phase Jitter		—	81	—	fs_{RMS}	Integration Range: 12 kHz to 20 MHz, Carrier: 622.08 MHz, T_A = +25°C
Rise/Fall Time (20% to 80%)	t_r/t_f	70	150	250	ps	—

Note 1: Measured with 400 mV signal, 50% duty cycle, all outputs loaded with 50Ω to V_{CC} – 2V, unless otherwise stated.

2: Specification for packaged product only.

3: Skew is measured between outputs under identical transitions.

4: See the Timing Diagram section.

5: Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = t_n – t_{n+1}$, where “t” is the time between rising edges of the output signal.

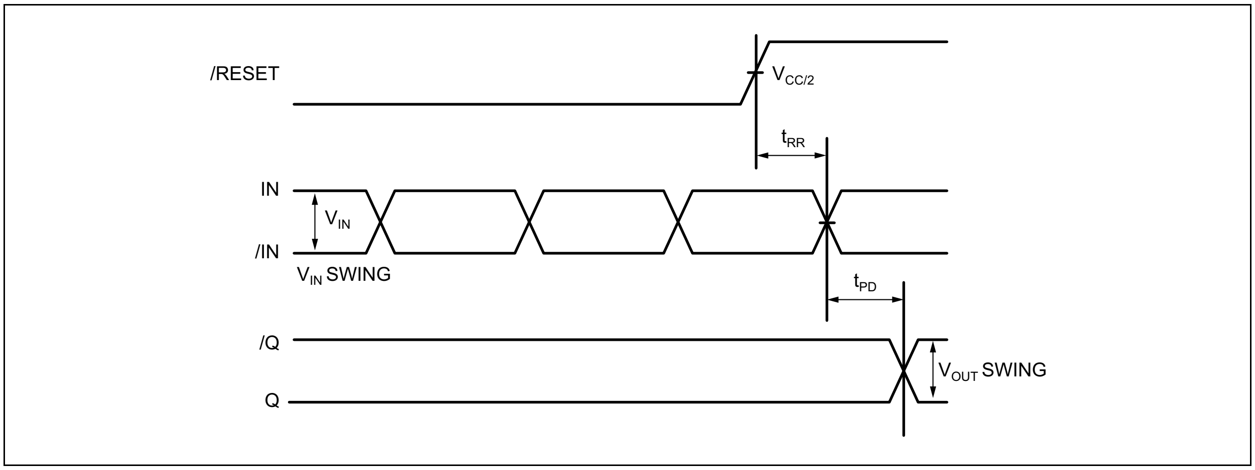
6: Total jitter definition: With an ideal clock input, of frequency ≤f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3x3 QFN-16Ld	θ_{JA}	—	60	—	°C/W	Still-air
	θ_{JA}	—	54	—	°C/W	500 lpfm
	ψ_{JB}	—	32	—	°C/W	Junction-to-board, Note 1

Note 1: Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Timing Diagram



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, V_{IN} = 400 mV, T_A = +25°C, unless otherwise stated.

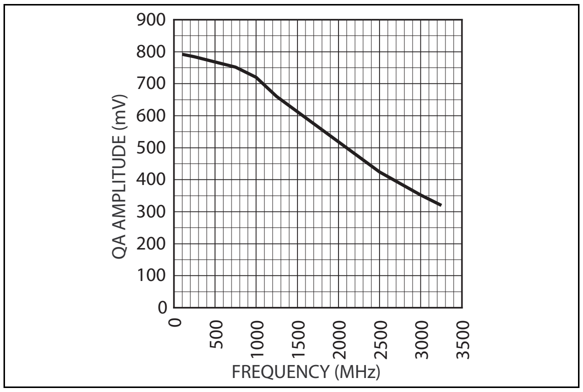


FIGURE 2-1: *QA Output Amplitude vs. Frequency.*

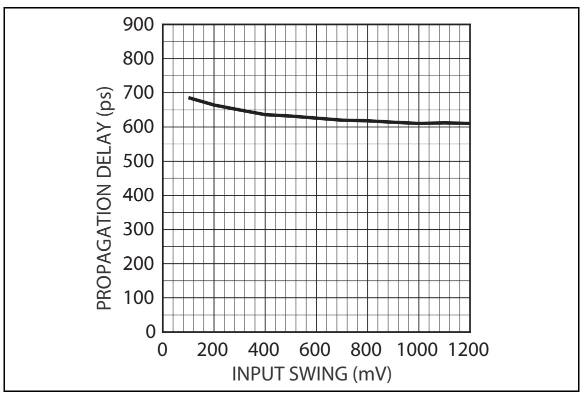


FIGURE 2-2: *IN-to-Q Propagation Delay vs. Input Swing.*

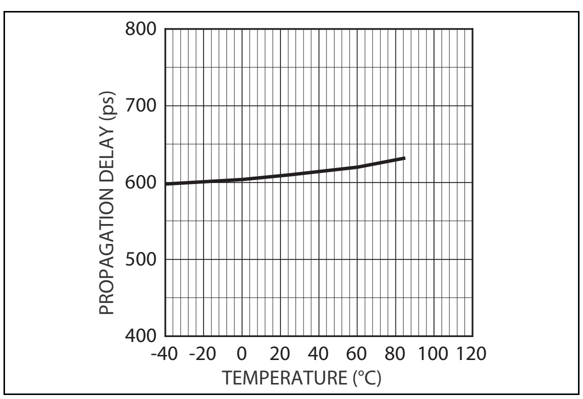


FIGURE 2-3: *IN-to-Q Propagation Delay vs. Temperature.*

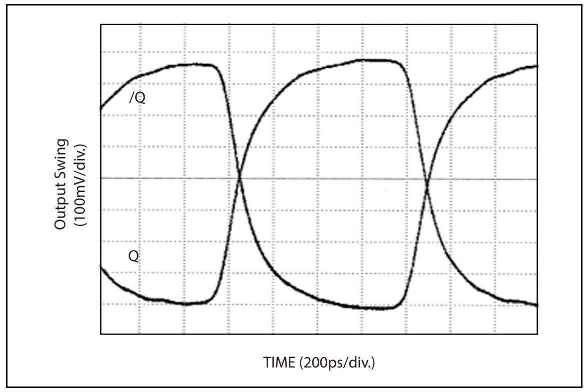


FIGURE 2-4: *622 MHz Output.*

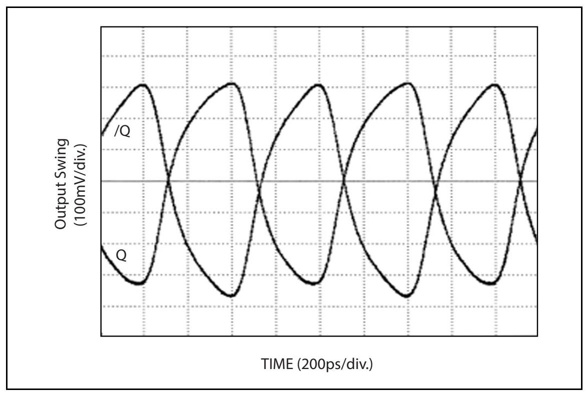


FIGURE 2-5: *1.25 GHz Output.*

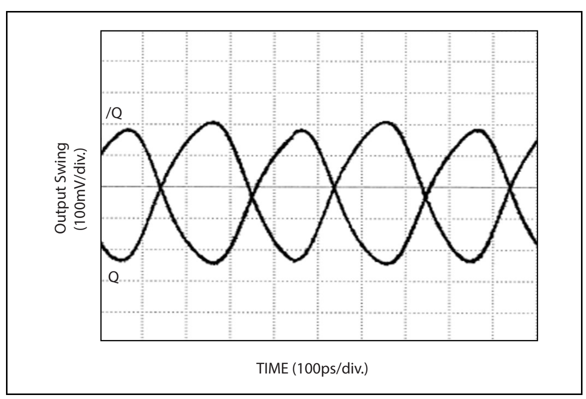


FIGURE 2-6: *2.5 GHz Output.*

3.0 ADDITIVE PHASE NOISE PLOT

Additive jitter is defined as the RMS Jitter of the device added to the input signal and is calculated in Equation 3-1.

EQUATION 3-1:

$$DeviceAdditiveJitter = \sqrt{OutputRMSJitter^2 - InputRMSJitter^2}$$

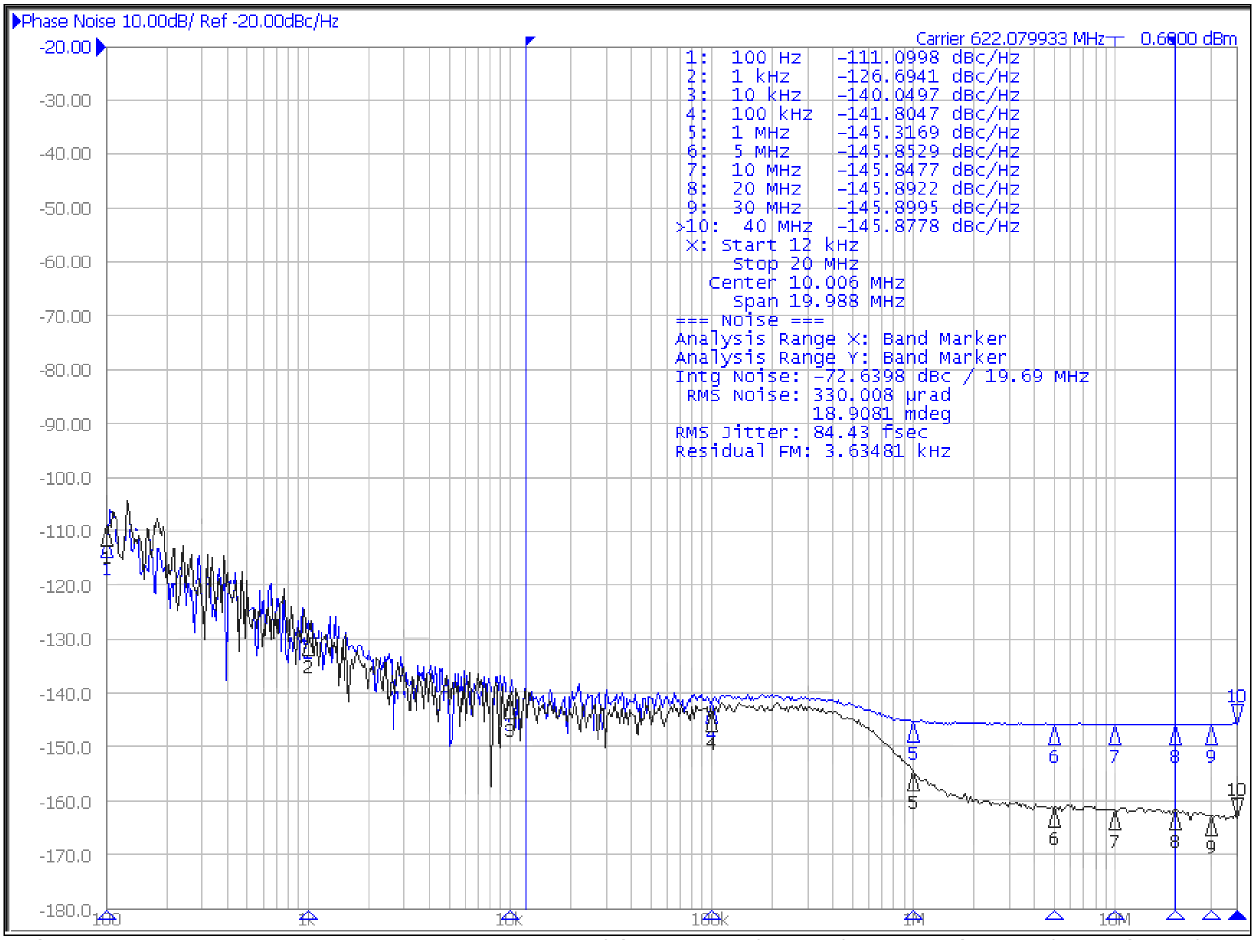


FIGURE 3-1: Integrated Phase Noise Plot of SY89874U (Device) and the Source (Input Signal).

From the plot shown in Figure 3-1, the device additive jitter can be calculated as follows.

EQUATION 3-2:

$$CalculatedAdditiveJitter = \sqrt{84.43^2 - 23.07^2} = 81.21fs$$

4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
12, 9	IN, /IN	Differential input. Internal 50Ω termination resistors to V_T input. Flexible input accepts any differential input. See the Input Interface Applications section.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential buffered LVPECL Outputs. Divided by 1, 2, 4, 8, or 16. See Truth Table. Unused PECL outputs may be left floating with no impact on jitter performance.
16, 15, 5	S0, S1, S2	Select pins. See Truth Table. LVTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected (divided by 16 mode). Input threshold is $V_{CC}/2$.
6	NC	No connect.
8	/RESET /DISABLE	LVTTL/CMOS logic levels. Internal 25 kΩ pull-up resistor. Logic high if left unconnected. Apply low to reset the divider (divided by 2, 4, 8, or 16 mode). Also acts as a synchronous disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is $V_{CC}/2$.
10	V_{REF-AC}	Reference voltage. Equal to V_{CC} – 1.4V (approximately). Used for AC-coupled applications only. Decouple the V_{REF-AC} pin with a 0.01 µF capacitor. See the Input Interface Applications section.
11	V_T	Termination center tap. For CML or LVDS inputs, leave this floating. Otherwise, see the figures within the Input Interface Applications section.
7, 14	V_{CC}	Positive power supply. Bypass with 0.1 µF//0.01 µF low-ESR capacitor.
13	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.

5.0 DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

Single-ended swing is defined as the amplitude of the signal when driven differentially. Differential swing is defined as IN – /IN (or Q – /Q).

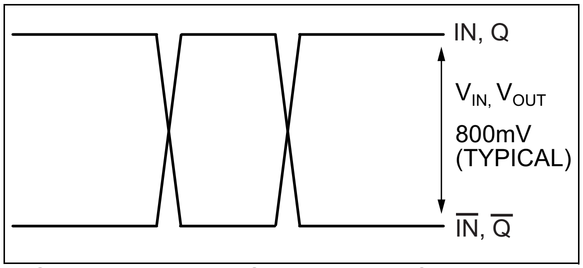


FIGURE 5-1: *Single-Ended Swing.*

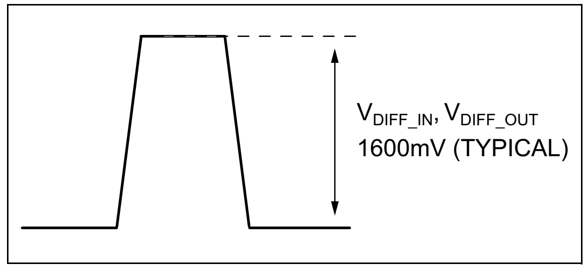


FIGURE 5-2: *Differential Swing.*

6.0 INPUT BUFFER STRUCTURE

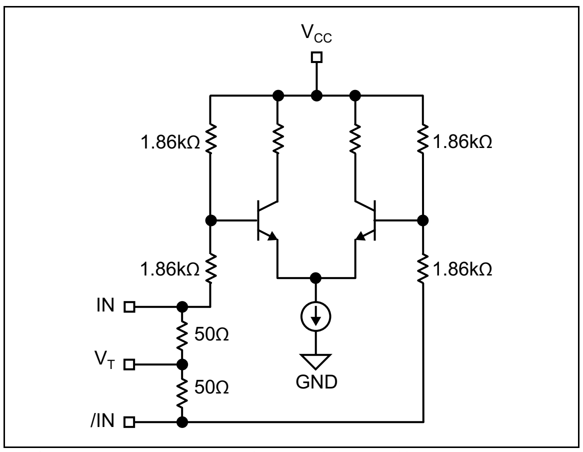


FIGURE 6-1: *Simplified Differential Input Stage.*

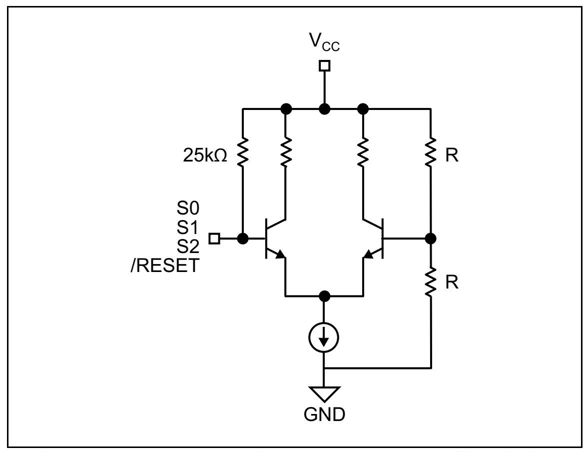


FIGURE 6-2: *Simplified LVTTL/CMOS Input Stage.*

7.0 INPUT INTERFACE APPLICATIONS

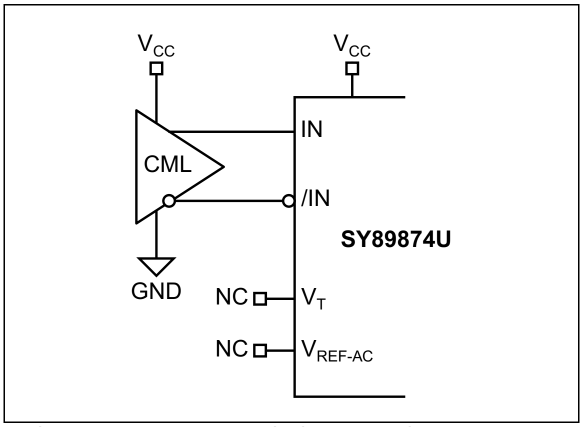


FIGURE 7-1: *DC-Coupled CML Input Interface.*

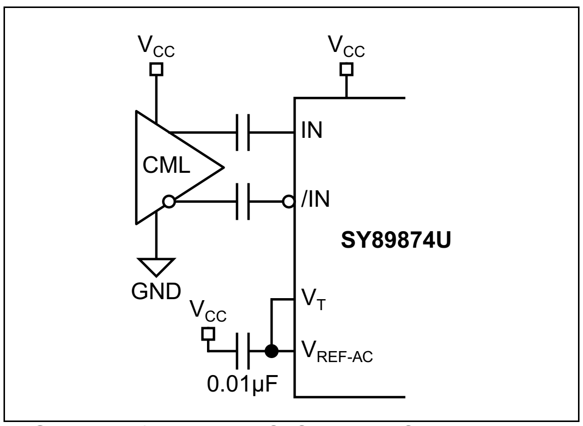


FIGURE 7-2: *AC-Coupled CML Input Interface.*

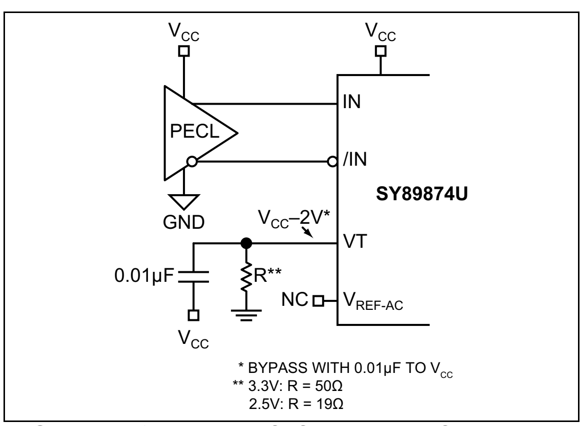


FIGURE 7-3: *DC-Coupled PECL Input Interface.*

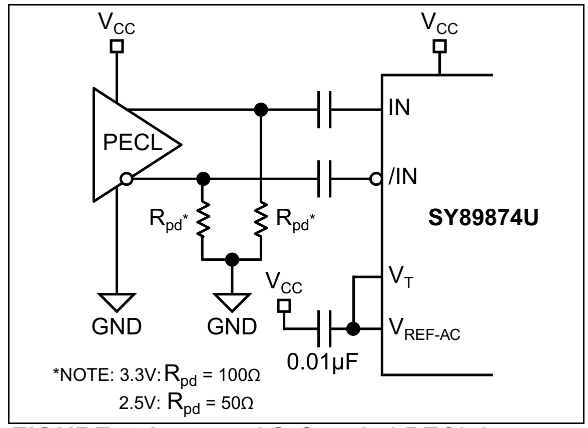


FIGURE 7-4: *AC-Coupled PECL Input Interface.*

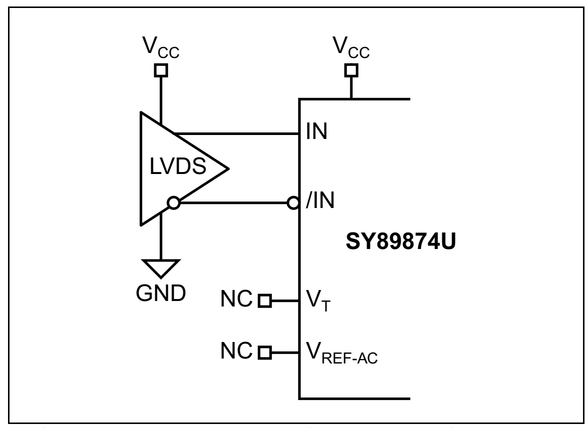


FIGURE 7-5: *LVDS Input Interface.*

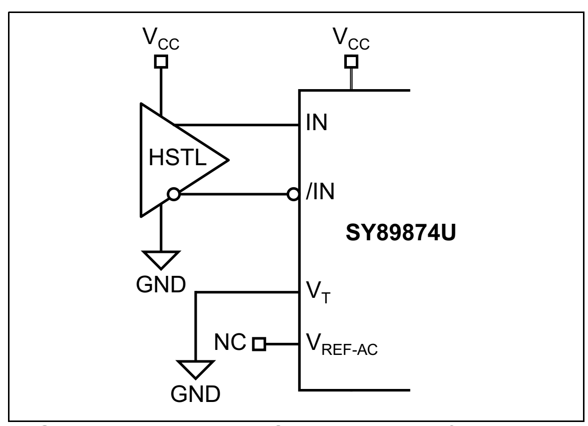


FIGURE 7-6: *HSTL Input Interface.*

8.0 LVPECL OUTPUT TERMINATION RECOMMENDATIONS

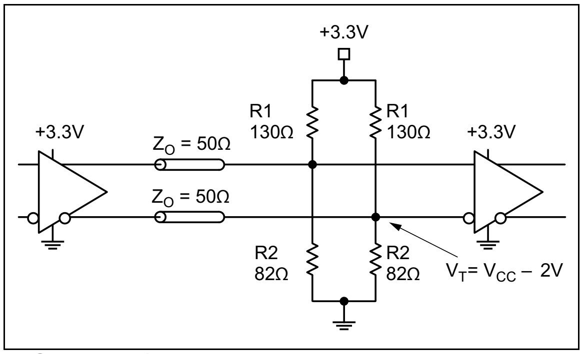


FIGURE 8-1: *Parallel Termination Thevenin Equivalent.*

For Figure 8-1, note that for +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

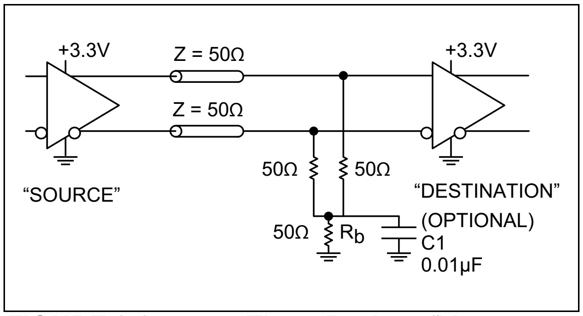


FIGURE 8-2: *Three-Resistor "Y Termination".*

For Figure 8-2, note that this is a power-saving alternative to Thevenin termination. Place termination resistors as close to destination inputs as possible. The R_b resistor sets the DC bias voltage, equal to V_T. For +3.3V systems R_b = 46Ω to 50Ω. For +2.5V systems, R_b = 39Ω. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

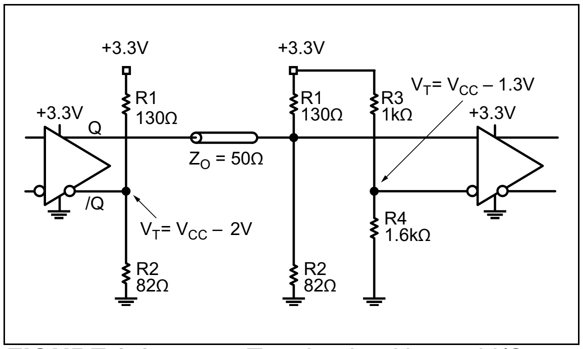


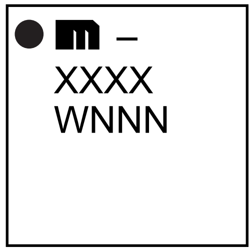
FIGURE 8-3: *Terminating Unused I/O.*

For Figure 8-3, note that the unused output (/Q) must be terminated to balance the output. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25 kΩ, R4 = 1.2 kΩ.

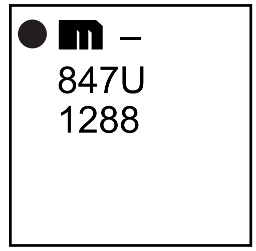
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

16-Lead QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

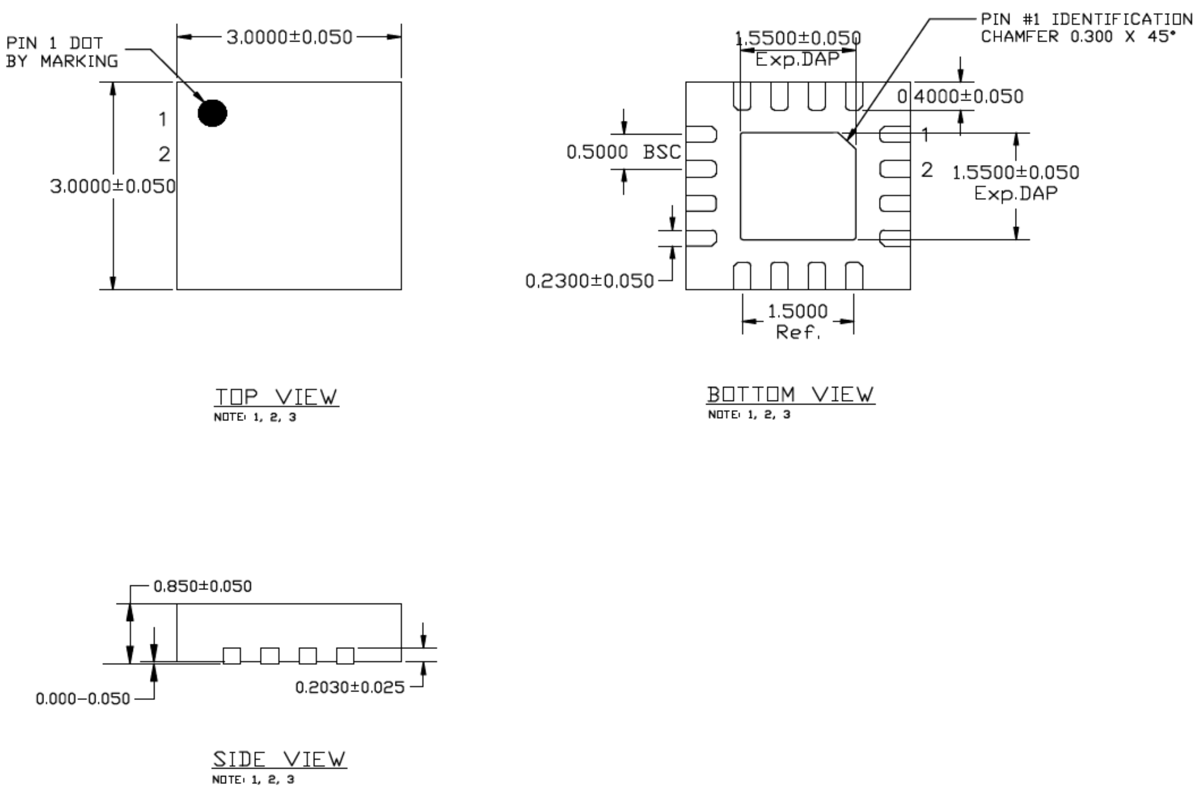
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

16-Lead 3 mm x 3 mm QFN Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN33-16LD-PL-1	UNIT	MM

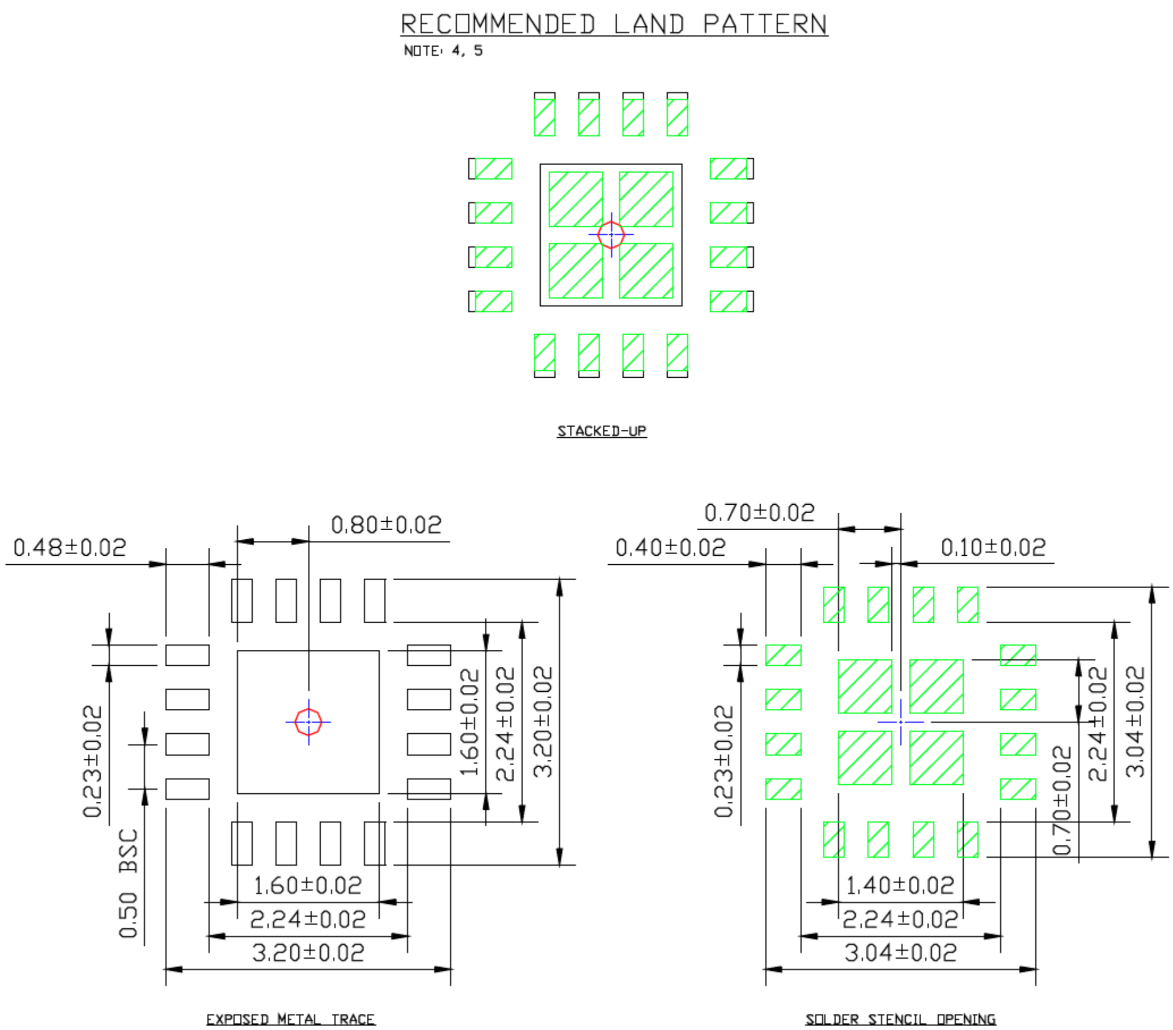


NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

Note: Package meets Level 2 moisture sensitivity classification and is shipped in dry-pack. Exposed pads must be soldered to a ground for proper thermal management.

POD-Land Pattern drawing # QFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document SY89874U to Microchip data sheet template DS20006108A.
- Minor text changes throughout.
- Added information about Additive Phase Jitter in AC Electrical Characteristics table and Additive Phase Noise Plot section.

Revision B (November 2018)

- Corrected units of measurement for Additive Phase Jitter in AC Electrical Characteristics from ps_{RMS} to fs_{RMS}.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Input Voltage	Package	Temperature Range	Tape and Reel

Device:	SY89874:	2.5GHz, Any Differential In-to-LVPECL, Programmable Clock Divider/Fanout Buffer with Internal Termination
Input Voltage:	U =	2.5V/3.3V
Package:	M =	3 mm x 3 mm QFN-16
Temperature Range:	G =	–40°C to 85°C (NiPdAu Lead-Free)
Special Processing:	<blank> = TR =	100/Tube 1,000/Reel

Examples:

a) SY89874UMG: SY89874, 2.5V/3.3V Input Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 100/Tube

b) SY89874UMG-TR: SY89874, 2.5V/3.3V Input Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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