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Keywords: Wafer Level Package, WLP, Flip Chip, Flip-Chip, CSP, Chip Scale Package, PCB Assembly, PCBA, Die Product, Silicon Circuit, Silicon Die Circuit

## APPLICATION NOTE 3377

# Maxim Wafer-Level Package Assembly Guide

Nov 12, 2004

*Abstract: Wafer-Level Packaging (WLP) allows an integrated circuit (IC) to be attached to a printed-circuit board (PCB) face-down, with the chip's pads connecting to the PCB pads through individual solder balls. This document describes the packaging technique and its advantages. It describes printed-circuit board (PCB) layout and assembly process development for Maxim WLP.*

Wafer-Level Packaging (WLP) uses individual solder balls to connect the integrated circuit (IC) to a printed-circuit board (PCB). The IC is mounted face-down. This technology differs from other ball-grid array, leaded, and laminate based CSPs because there are no bond wires or interposer connections. The principle advantage is that IC-to-PCB board inductance is minimized. Secondary benefits are reduction in package size and manufacturing cycle time, and enhanced thermal conduction characteristics.

This document describes printed-circuit board (PCB) layout and assembly process development for Maxim WLP. Note that it is intended for initial PCB layout design and assembly process development and does not assume any reliability objective for the customer end product. Customers still need to qualify their specified end product life reliability requirements.

## Package Construction

### Maxim Package Outlines

The WLP solder bump interconnect is manufactured by building-up on a silicon wafer substrate. A film of BCB (Benzocyclobutene) resin is applied over the wafer circuit surface. This film provides mechanical stress relief for the ball attachment and electrical isolation at the die surface. Vias are imaged in the BCB film, providing electrical contact to the IC bond pad. A UBM (Under Bump Metal) layer is added over vias. Typically, a second application of BCB serves as a solder mask to define the diameter and position of reflowed solder balls. Current package I/O designs include from two up to fifty-five solderable terminals, see **Figure 1**. Standard solder bump alloys are eutectic Sn63Pb37, "High-Pb" Pb95Sn5, and "Pb-Free" Sn96.5Ag3Cu0.5. A cross-section of a single WLP solder bump structure is shown in **Figure 2**. The backside of the component is bare silicon with a laser inscribed Pin-1 designator and identification code. A double metal layer redistribution (RDL) process allows for moving solder bumps from peripheral bond pads to any bump array pattern.

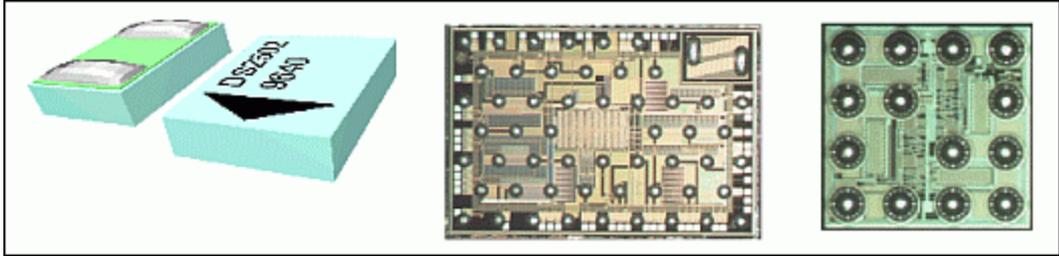


Figure 1. Generic 2-Bump CSP, 55-Bump Flip Chip, 4 x 4 UCSP™.

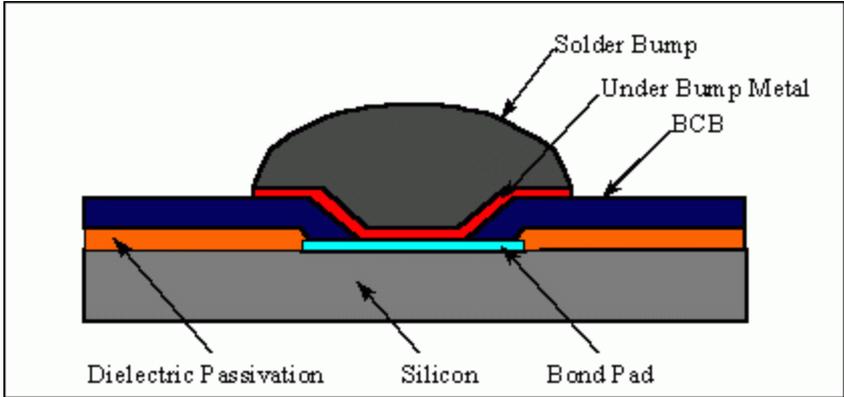


Figure 2. Cross-section diagram of generic WLP construction.

### WLP Carrier Tape

All WLPs are shipped in tape-and-reel (T&R) format only. Tape-and-reel requirements are based on EIA-481 and EIA-746&747 standards. A typical tape-and-reel construction is shown in **Figure 3**. All Maxim Flip Chip and CSP devices are supplied in embossed pocketed carrier tape with pressure seal adhesive (PSA) cover tape in 7in or 13in reel format. Other type carrier tapes such as Surftape® or Surftape-Lite®, and other reel sizes may be available upon request.

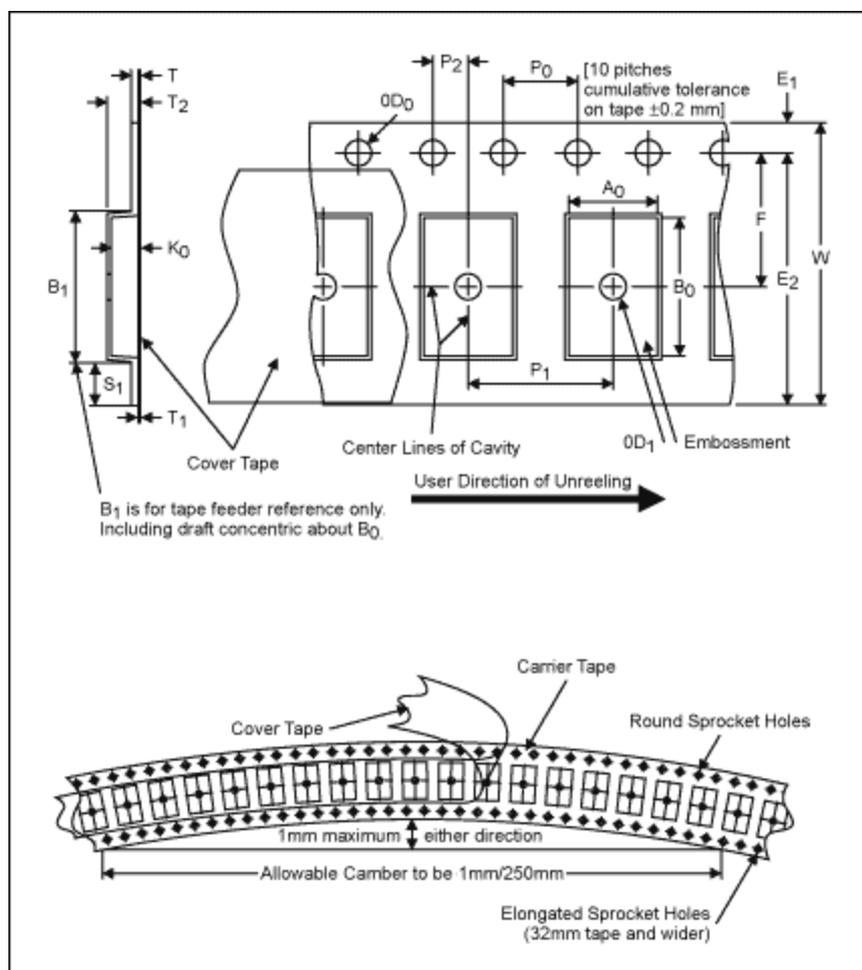


Figure 3. Typical WLP carrier tape construction.

Balls are facing down in the tape-and-reel carrier. Pin 1 orientation is consistent in each pocket in the carrier tape. The cover tape shall exhibit a total peel strength from 0.1N to 1.0N (10gf to 102gf calibrated scale reading).

## PCB Layout

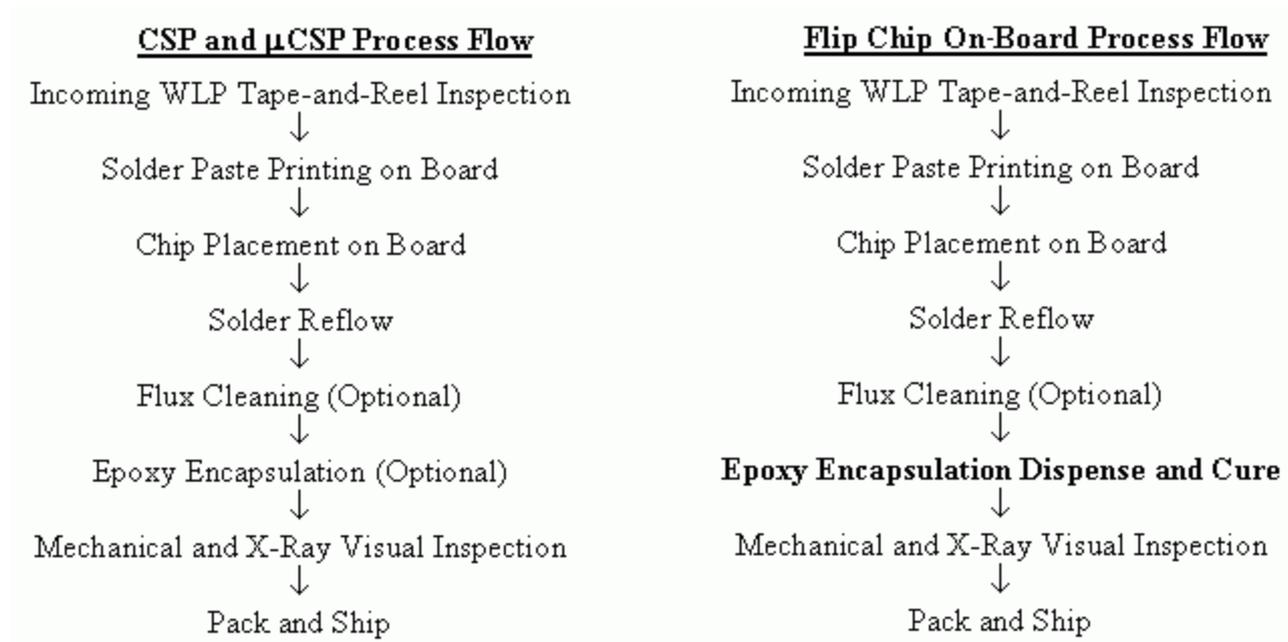
PCB design requirements are based on IPC-A-600 and IPC-6012A standards. Standard FR4 ( $T_g = 120^\circ\text{C}$  to  $150^\circ\text{C}$ ) copper clad laminate may be utilized for all solder reflow profiles up to  $240^\circ\text{C}$  peak temperature, with high-performance FR4 or BT laminate ( $T_g = 170^\circ\text{C}$  to  $185^\circ\text{C}$ ) recommended for solder reflow profiles from  $240^\circ\text{C}$  to  $270^\circ\text{C}$  peak temperatures. Electroless Nickel-Immersion Gold (ENIG) is the preferred plating for the PCB copper land pads surface finish (minimum 3 microinch/maximum 20 microinch Au over a minimum 100 microinch/maximum 300 microinch Ni) for all Maxim solder bump alloys. Organic surface protective (OSP) coating over copper land pads is also acceptable.

Non-Solder-Mask Defined (NSMD) land pads are always preferred over Solder-Mask Defined (SMD) pads for all solder bump grid array packages. Solder mask is recommended between all pads, with solder mask design clearance to pads of 0.002in to 0.003in. Pad sizes for collapsible solder bump reflow (eutectic Sn-Pb and Pb-Free) is normally 20 to 25% less than the solder bump maximum diameter, which enables the resultant solder joint to achieve a maximum component standoff height. Pad sizes for non-collapsible solder bump reflow

(High-Pb) is normally 0.002in to 0.004in greater than the solder bump maximum diameter, which enables X-Ray inspectability for solder wetting and solder joint acceptance. The only exceptions to this "High-Pb" solder bump pad design rule are the Maxim 2-Bump CSPs (Figure 1), for which the recommended land patterns are 1:1 with the maximum bump dimensions, in order to minimize their inherent bump design die tilt which occurs during solder reflow. Land patterns may be either circular or square. Pads and connecting traces should be arranged symmetrically to prevent off-center wetting forces during solder reflow. To prevent solder thieving, each NSMD copper pad should be connected by only one signal trace, the trace width being no more than 1/2 the diameter of its connected NSMD copper pad.

All WLP component PCB locations should be selected so that adjacent components may include much taller packages that can shroud the WLP and provide protection from potential contact damage.

## PCB Assembly Process Flow



## Solder Paste Screen Print Process

Solder paste screen print process control is critical to the PCB assembly yield and solder joint interconnections reliability. Inspection for paste height, percent pad coverage, and registration accuracy to solderable land patterns is mandatory.

- Solder Paste Selection: Use Type 3 (25 to 45 micron solder sphere particle size) or Type 4 (20 to 38 microns), depending on solder stencil aperture size limitations. It is recommended that a low halide (< 100ppm halides) No-Clean rosin/resin flux system, J-STD-004 designation ROL0/REL0, be used to eliminate post-reflow assembly cleaning operations.
- Solder Stencil Fabrication: Use Laser Cut stainless steel foil with electro-polishing or Nickel base metal electroformed foil processes. The Nickel E-form process is more expensive but offers the most repeatable solder paste deposition from ultra small apertures, and has the advantage of being formed to any customer required stencil thickness. The stencil openings with trapezoidal cross section from these fabrication processes also enhance the solder paste release.
- Solder Stencil Aperture Design: Use aperture aspect ratio of  $\geq 0.75$  for Laser Cut SS and  $\geq 0.66$  for E-

Form Ni, with square (25 micron corner radius) vs. round aperture preferred for improved solder paste deposition repeatability. Aperture aspect ratio is defined as the aperture opening area divided by the aperture side wall surface area. Optionally, apertures X and Y offsets from land pads may be utilized to maximize separation between paste deposits and minimize the potential for solder bridging, as in **Figures 4 and 5**.

- Solder Stencil Thickness: Solder stencil thickness should not exceed the solder bump height. Solder stencil thickness must achieve the aperture aspect ratio requirements in combination with the selected aperture design. When these stencil design requirements conflict with other required SMT components in a mixed technology PCB assembly, a step-down stencil or two-print stencil process may be utilized in compliance with IPC-7525 design standards.

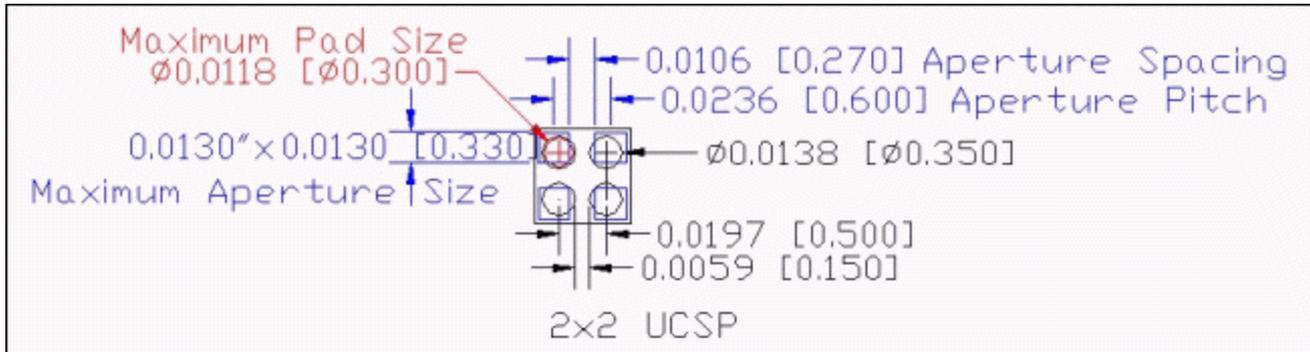


Figure 4. Example of 2 x 2 UCSP offset apertures Solder Stencil design.

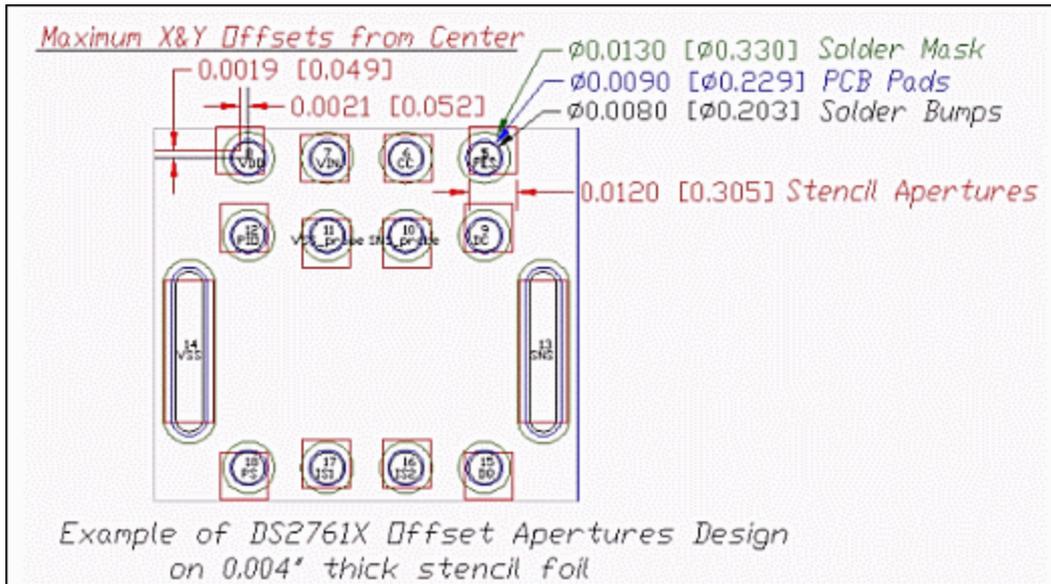


Figure 5. Example of DS2761X Flip Chip offset apertures Solder Stencil design.

## Component Placement

All Maxim WLP silicon die may be picked up by vacuum nozzles from pocketed carrier tape reels and placed onto PCB substrates using standard automated fine pitch IC Pick-and-Place machines with  $\leq 0.050\text{mm}$  placement accuracy at  $4\sigma$ . Stationary Tape-and-Reel feeder bases are also required for all Pick-and-Place systems. Systems using mechanical centering pick devices are not acceptable due to the high potential for

mechanical damage to the silicon package.

- The placement accuracy of the automated Pick-and-Place system is also dependent on its vision alignment of package outline centering vs. bump grid array centering. Package outline centering is employed for higher speed placement with reduced alignment accuracy requirements, and bump grid array vision centering is employed for maximum alignment accuracy at lower placement rates. The maximum package outline centroid x,y design tolerance from bump grid array centroid position is  $\pm 0.035\text{mm}$ .
- Maximum recommended allowable solder bump placement offset from PCB pad center to assure self-centering alignment from solder reflow wetting forces is  $\pm 0.100\text{mm}$  in X and Y directions.
- All silicon die package contact forces should be controlled to  $\leq 2\text{N}$  (204gf). Actual placement forces should be measured periodically using a calibrated load cell with meter.
- 2D transmission X-Ray inspection is required for placement accuracy verification and measurement.

## Solder Paste Reflow

The Maxim's WLPs are compatible with industry standard solder reflow processes. Nitrogen inert atmosphere reflow soldering is optional.

- Forced gas convection reflow ovens are recommended for controlled heat transfer rates throughout the process.
- WLP solder bump components are qualified for up to three standard reflow cycles.
- 2D Transmission X-Ray or 3D X-Ray Laminography is recommended as a post-reflow solder joint inspection sample monitoring method for solder shorts, insufficient solder, voids within the solder joint, and potential solder opens.
- Eutectic Sn-Pb solder paste reflow to eutectic Sn-Pb and "High-Pb" solder bump WLPs: Nominal peak temperature is  $220^{\circ}\text{C} \pm 15^{\circ}\text{C}$  with time above the  $183^{\circ}\text{C}$  melting point of  $60\text{s} \pm 15\text{s}$ , which should be verified at machine setup by inline thermocouple measurements oven profiling. A typical eutectic Sn-Pb solder paste reflow temperature profile is shown in **Figure 6**. The peak temperature Upper Limit is recommended for eutectic Sn-Pb solder paste reflow to "High-Pb" solder bump WLP, to further enhance the intermetallic bond layer at the bump interface.

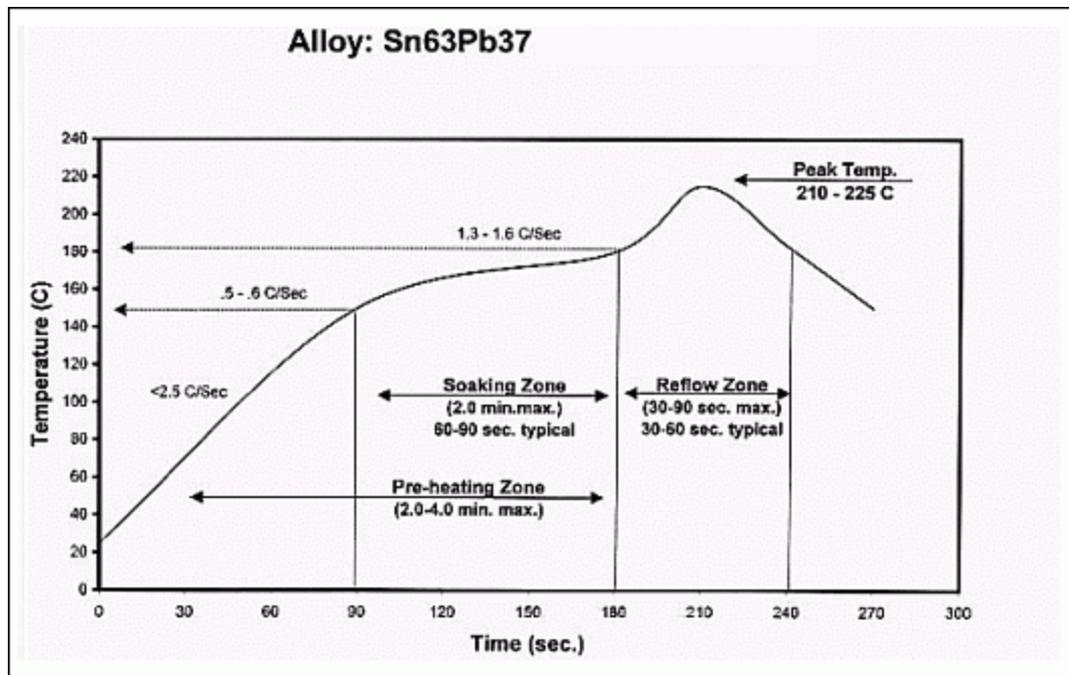


Figure 6. Typical temperature Profile for Eutectic Sn-Pb Solder paste.

- "Pb-Free" solder paste reflow: Nominal peak temperature is  $250^{\circ}\text{C} \pm 10^{\circ}\text{C}$  with time above the  $217^{\circ}\text{C}$  to  $221^{\circ}\text{C}$  melting point of  $60\text{s} \pm 15\text{s}$ , which should be verified at machine setup by inline thermocouple measurements oven profiling. A typical "Pb-Free" solder paste reflow temperature profile is shown in **Figure 7** for Sn96.5Ag3.5 and SnAg(2-4)Cu(0.5-0.8) alloys.

More information on Pb-Free.

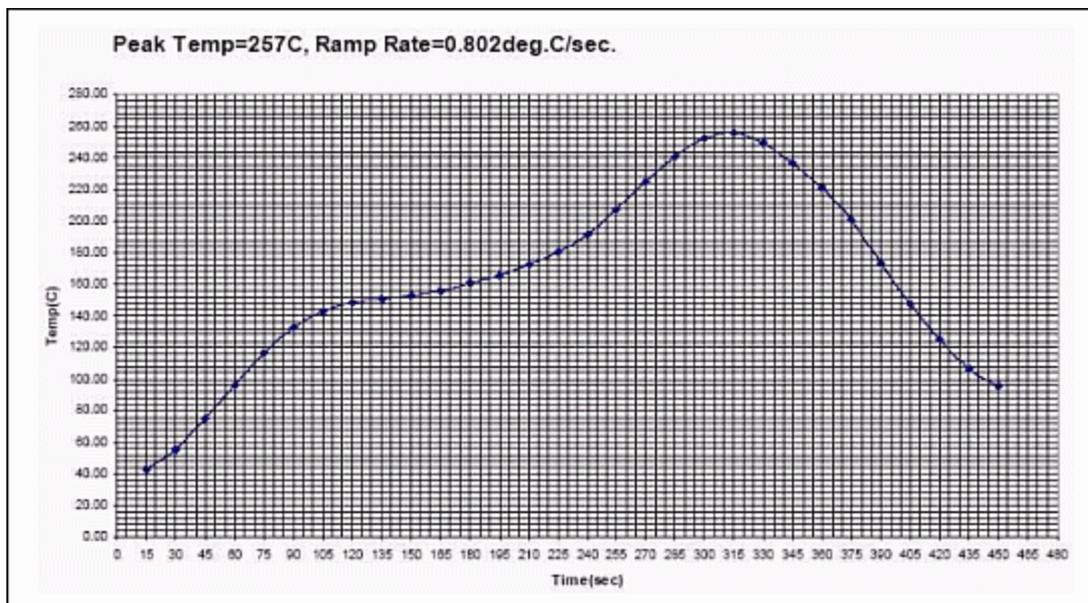


Figure 7. Typical temperature profile for Sn96.5Ag3.5 and Sn-Ag-Cu "Pb-Free" solder paste.

## Component Rework

WLP rework utilizes the same process as for reworking a typical ball-grid array (BGA).

- WLP removal uses localized heating comparable to the original reflow profile, employing a hot gas convection chimney nozzle and bottom-side preheat.
- Once the nozzle temperature exceeds the solder joint melting point, the defective part can be removed using plastic tweezers or vacuum tool.
- The PCB pads must be resurfaced using a temperature-controlled soldering iron.
- Gel or tacky flux is then applied to the pads.
- A replacement part is picked up with a vacuum needle pick-up tool and accurately placed using a vision alignment placement jig.
- Reflow the part using the same hot gas convection nozzle and bottom-side preheat, in accordance with the original reflow profile specifications.

## Epoxy Encapsulation (Required for all Flip Chip On Board Assemblies)

Capillary Underfill epoxy and/or Glob-Top epoxy encapsulation may be added to the assembled CSP circuit to increase mechanical strength of the solder joint interconnections and provide accelerated thermal cycle (ATC) test reliability enhancement up to 10X over components without epoxy encapsulation. This "encapsulation effect" results in enhanced performance from the mechanical coupling mechanism of epoxy adhesive between chip and substrate. Epoxy encapsulation also provides a physical barrier to moisture, humidity, and chemical contamination. In addition, Underfill epoxy provides a physical barrier to solder creep from thermal cycle stress between adjacent solder bumps, and Glob-Top epoxy provides physical protection from mechanical contact damage to the backside silicon surface and edges of the WLP.

## Material Property Considerations

- Cured Epoxy Coefficient of Linear Expansion (CTE) match to Solder Joint interconnects, Sn63Pb37 (21ppm/°C) - Pb95Sn5 (29ppm/°C), 65% to 70% silica filler.
- High Glass Transition (Tg) to achieve all product storage life temperature requirements (Minimum Cured Epoxy Tg ≥ Substrate Tg; FR4 = 120°C to 135°C, BT/Enhanced FR4 = 170°C to 185°C).
- High adhesion properties to BCB passivation and to LPI solder masks.
- Low Ionics < 100ppm total Halides.
- Low Viscosity and Fast Flow rate, with flow capability to 50mm (2mil) minimum gap size.
- Low warpage, low shrinkage matrix.
- Minimal moisture absorption.

## Visual Inspection Acceptance Criteria

- Underfill epoxy must achieve a continuous positive fillet around the entire perimeter of the die with no voids allowed. A positive fillet is defined as having a minimum contact height to the bottom side edge of the die and a maximum contact height not to exceed the topside edge of the die. In addition, the fillet must demonstrate a positive wetting angle away from the outside die edges to the substrate surface.
- The visible epoxy surface area must be uniform and free of voids and pinholes.
- Epoxy shall not adjoin to any assembly required electrical contact surfaces.

Vertical Scanning Acoustic Microscopy (C-SAM) Imaging may be utilized as an Analytical Method for Voids in Underfill Detection, as shown in **Figures 9** and **10**.

- Liquid Epoxy Dispense weight gain measurement may be employed as a simple method of monitoring SPC capability.

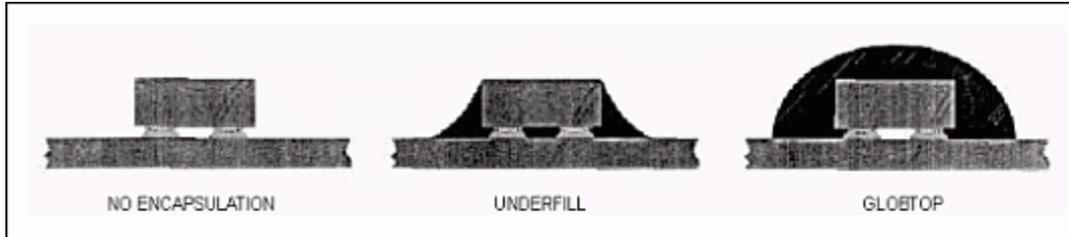


Figure 8. Epoxy encapsulation options.

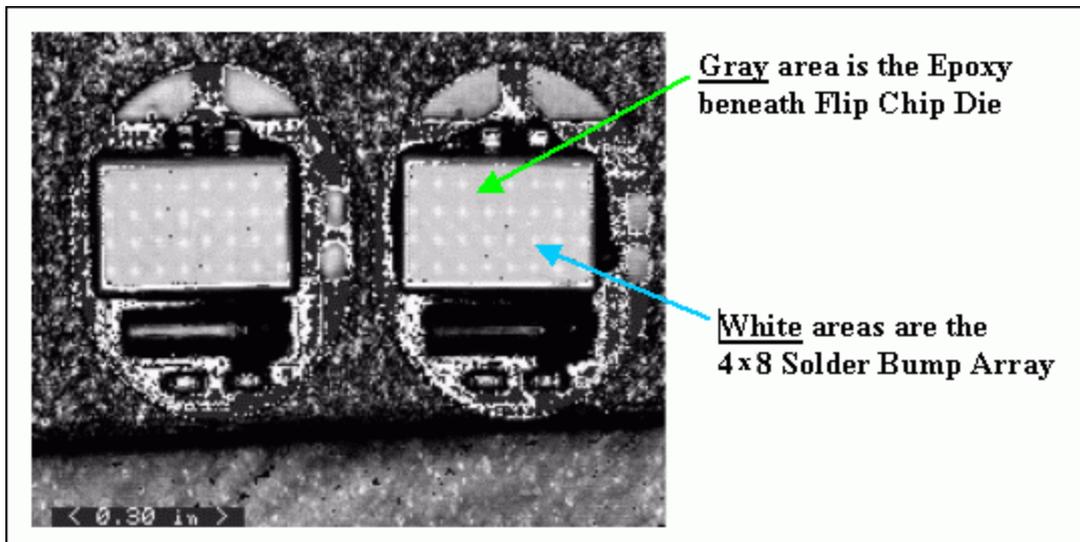
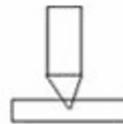
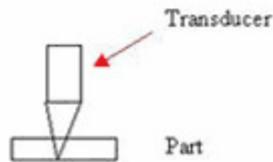
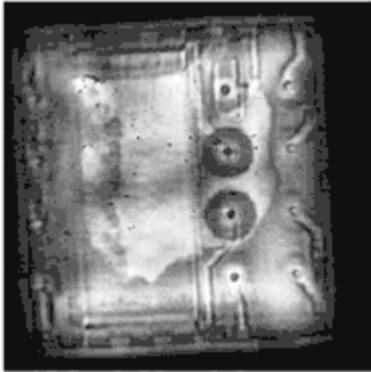


Figure 9. Example of vertical scanning acoustic microscopy (C-SAM) imaging.

**FA STEP:** Inspection of die using Ultrasound and two different focal point transducers.  
**SHOWING:** The die to ball interface. The light area in the center of the die indicates there is no underfill.

Transducer: UHF MHz 8 mm  
Resolution: 10  $\mu$ m x 10  $\mu$ m

Transducer: UHF MHz 5.9 mm  
Resolution: 10  $\mu$ m x 10  $\mu$ m



The first image was produced with a UHF, 8 mm transducer, and there are some bright areas which are indicative of air. It is not clear if this is due to the presence of a delamination at the die-underfill interface, or a lack of underfill at these locations.

The schematic above demonstrates the fact that a longer focal length transducer can focus at deeper interfaces. In this case, since the die was 700 microns, a UHF, 8 mm transducer produced better images. A short focal length transducer may not be able to reach down to deeper interfaces, and should therefore be used for thinner die (450-600 microns approximately). UHF transducers with shorter focal lengths (2,3,4mm ) should be used for die that are less than 400-450 microns thick.

Figure 10. Example of vertical scanning acoustic microscopy (C-SAM) imaging.

## Pack and Ship

To prevent damage to the WLP component, care must be taken in handling, packing, and shipping WLP assemblies, especially when the WLP is mounted without epoxy encapsulation. The assembly site's packing specifications for PCB mounted with WLP must be reviewed and optimized.

UCSP is a trademark of Maxim Integrated Products, Inc.

### Related Parts

DS1804	Nonvolatile Trimmer Potentiometer	Free Samples
DS1845	Dual NV Potentiometer and Memory	Free Samples
DS2401	Silicon Serial Number	Free Samples
DS2406	Dual Addressable Switch Plus 1Kb Memory	Free Samples
DS2411	Silicon Serial Number with V <sub>CC</sub> Input	Free Samples
DS2415	1-Wire Time Chip	
DS2417	1-Wire Time Chip With Interrupt	Free Samples
DS2432	1Kb Protected 1-Wire EEPROM with SHA-1 Engine	Free Samples
DS2433	4Kb 1-Wire EEPROM	
DS2502	1Kb Add-Only Memory	Free Samples
DS2760	High-Precision Li+ Battery Monitor	
DS2761	High-Precision Li+ Battery Monitor	
DS2762	High-Precision Li+ Battery Monitor with Alerts	Free Samples
DS60	Analog Temperature Sensor	
DS9503	ESD Protection Diode with Resistors	Free Samples

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