Keywords: Clock Rate Adapter, Clock Adapter, CLAD, LIU, Line Interface Unit, T3, E3, ATM, Packet PHYs, DS3251, DS3252, DS3253, DS3254, DS3161, DS3162, DS3163, DS3164, DS3166, DS3168, DS3162, DS3171, DS3172, DS3173, DS3174, DS3181, DS3182, DS3183, DS3184

APPLICATION NOTE 3609

Clock-Rate-Adapter (CLAD) Features for DS325X, DS316X, DS317X, and DS318X

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Abstract: This application note describes how to configure the clock-rate-adapter (CLAD) functions in DS325X, DS316X, DS317X, and DS318X devices to create multiple clock sources. Depending on the application, these sources can be used as LIU reference or transmit clocks.

Introduction

This application note describes how to configure the clock-rate-adapter (CLAD) functions to create multiple clock sources. These sources can be used as LIU reference clocks or transmit clocks by the DS325X, DS316X, DS317X, and DS318X devices.

This application note applies to the following products.

T3/E3 LIUs	T3/E3 ATM/Packet PHYs	T3/E3 SCTs	T3/E3 ATM/Packet PHYs with LIUs
DS3251	DS3161	DS3171	DS3181
DS3252	DS3162	DS3172	DS3182
DS3253	DS3163	DS3173	DS3183
DS3254	DS3164	DS3174	DS3184

Using the CLAD in the DS325X

The clock-rate-adapter block for the DS325X T3/E3 LIUs generates all the required clock rates from a single input clock. If a single transmission-quality clock source (DS3, E3, or STS-1) is present, the clock-rate adapter can synthesize the transmission-quality clocks at the other two line rates. Both the input clock and synthesized clocks are then available for use as master clocks by the clock/data recovery (CDR) blocks and jitter attenuators. Operating from the LIU's master clock, the CDR block takes the amplified, equalized signal from the AGC/equalizer block and produces separate clock, positive data, and negative data signals. In hardware mode, the clock-rate adapter is entirely controlled by the T3MCLK, E3MCLK, and STMCLK pins.

In CPU bus mode, additional clock-rate-adapter control options are available in the CACR register. When the Alternate Master Clock Enable (AMCEN) control bit is set to 1, the clock-rate-adapter block is

configured for alternate master clock mode. In this mode, the clock-rate adapter expects to receive a clock whose frequency is specified by the Alternate Master Clock Select (AMCSEL) control bits rather than by a DS3, E3, or STS-1 clock. Valid input frequencies for the alternate master clock are 19.44MHz, 38.88MHz, and 77.76MHz. In alternate master clock mode, the clock-rate adapter can synthesize up to two of the three clock rates: DS3, E3, or STS-1. To synthesize the DS3 and E3 clocks, the alternate master clock should be applied to the STMCLK pin. To synthesize the DS3 and STS-1 clocks, the clock should be applied to the E3MCLK pin, and applied to the T3MCLK pin to synthesize the E3 and STS-1 clocks.

The DS325X device can be powered up with an alternate clock applied to one of the MCLK pins, even though the power-on default values of AMCEN and AMCSEL[1:0] may not match the applied clock. Once these control bits are properly configured after power-up, the clock-rate adapter begins to synthesize the proper master clocks. The device, as a whole, functions normally.

CPU bus mode can also output a synthesized master clock on the T3MCLK, E3MCLK, and STMCLK pins for use by neighboring framers, mappers, and other components. To output the synthesized DS3 master clock on T3MCLK, set CACR:T3MOE = 1. To output the synthesized E3 master clock on E3MCLK, set CACR:E3MOE = 1, or set CACR:STMOE = 1 to output the synthesized STS-1 master clock on STMCLK.

The CLAD Configuration Registers for DS325X

The clock-rate-adapter control register required to configure the CLAD is described below.

Register Name: **CACR**
Register Description: **Clock-Rate-Adapter Control Register**
Register Address: **08h**

Bit	7	6	5	4	3	2	1	0
Name	T3MOE	E3MOE	STMOE	—	—	AMCSEL[1]	AMCSEL[0]	AMCEN
Default	0	0	0	0	0	0	0	0

Bit 7: T3MCLK Output Enable (T3MOE). When the clock-rate-adapter block is configured to synthesize the DS3 master clock, the DS3 master clock can be output on the T3MCLK pin by setting T3MOE = 1. This clock can then be used as the transmit clock for neighboring DS3 framers and other components requiring a DS3 clock. This bit should only be set to 1 if the T3MCLK pin is not driven externally.

0 = T3MCLK output driver disabled
1 = T3MCLK output driver enabled

Bit 6: E3MCLK Output Enable (E3MOE). When the clock-rate-adapter block is configured to synthesize the E3 master clock, the E3 master clock can be output on the E3MCLK pin by setting E3MOE = 1. This clock can then be used as the transmit clock for neighboring E3 framers and other components requiring an E3 clock. This bit should only be set to 1 if the E3MCLK pin is not driven externally.

0 = E3MCLK output driver disabled
1 = E3MCLK output driver enabled

Bit 5: STMCLK Output Enable (STMOE). When the clock-rate-adapter block is configured to synthesize the STS-1 master clock, the STS-1 master clock can be output on the STMCLK pin by setting STMOE = 1. This clock can then be used as the transmit clock for neighboring SONET framers, mappers, and

other components requiring an STS-1 clock. This bit should only be set to 1 if the STMCLK pin is not driven externally.

0 = STMCLK output driver disabled
1 = STMCLK output driver enabled

Bits 2 to 1: Alternate Master Clock Select (AMCSEL[1:0]).

00 = 19.44MHz
01 = 38.88MHz
10 = 77.76MHz
11 = Undefined

Bit 0: Alternate Master Clock Enable (AMCEN).

0 = alternate master clock mode disabled
1 = alternate master clock mode enabled

Using the CLAD in the DS316X, DS317X, and DS318X

The CLAD in the DS316X, DS317X, and DS318X devices is used to create multiple internal clock frequencies (DS3, E3, or STS-1) from a single clock-reference input on the CLKA pin. The clock frequency applied to CLKA must be one of the following:
1. DS3 (44.736MHz)
2. E3 (34.368MHz)
3. STS-1 (51.84MHz)

If one of these clocks is present, the other two clocks can be generated. If necessary, the internally generated clocks can be driven on output pins CLKB and CLKC for external use.

Configuring the CLAD in the DS316X, DS317X, and DS318X
If using the DS317X or DS318X's LIU, the CLAD supplies the clock to the receive LIU of DS317X or DS318X. The CLAD of DS316X, DS317X, and DS318X are configured by the CLAD bits in the GL.CR2 register. In this case, the user must supply a DS3, E3, or STS-1 clock to the CLKA pin.

The user must supply at least one of the three frequency rates (DS3, E3, or STS-1) to the CLKA pin. The CLAD[3:0] bits inform the PLL of the frequency applied to the pins. **Figure 1** shows the CLAD block for the DS316X, DS317X, and DS318X.
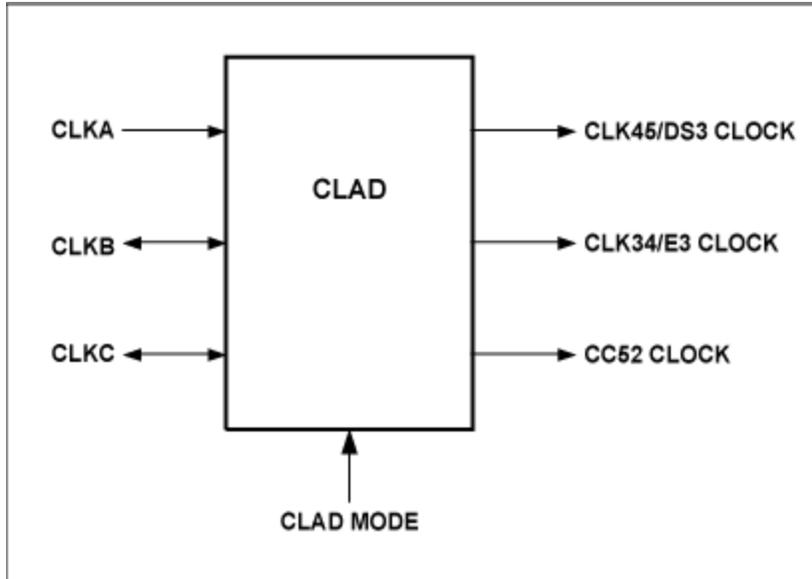
Figure 1. CLAD block for the DS316X, DS317X, and DS318X.

The FM bits (located in **PORT.CR2**; see below) control the selection of the output clock of the CLAD applied to the LIU and to the transmitter. The CLAD provides maximum flexibility. The application may supply any of the three clock frequencies and use the CLAD to provide the remaining frequencies required.

The CLAD can also be disabled and all three clocks supplied externally using the CLKA, CLKB, and CLKC pins as inputs. When the CLAD is disabled, the three reference frequencies of DS3, E3, and STS-1 must be applied to the CLKA, CLKB, and CLKC pins, respectively. If any of the three frequencies is not required, it does not need to be applied to the CLAD clock pins.

The CLAD MODE inputs to the CLAD are composed of CLAD[3:0] control bits (located in the GL.CR2 register) which determines which pins are input and output and which clock rate is on which pin. Please see **Table 1** below for more details.

When CLAD[3:0] = 00XX, the PLL circuits are disabled and the signals on the input clock pins CLKA, CLKB, and CLKC are used as the internal LIU reference clocks. When CLAD[3:0] = (01XX, or 10XX, or 11XX), then none, one, or two PLL circuits are enabled to generate the required clocks, as determined by the CLAD[3:0] bits, the framing mode (FM[5:0]), and the line mode control bits (LM[2:0]) located in **PORT.CR2**.

The Line Mode bits select the main port interface-operational modes. If a clock rate is not required on the CLAD output clock pins or for the LIU's reference clock, then the PLL used to generate that clock is disabled and powered down.

The CLAD Configuration Registers for DS316X, DS317X, and DS318X
The two registers required to configure the CLAD are described below.

Register Name: **GL.CR2**
Register Description: **Global Control Register 2**
Register Address: **004h**

Bit #	15 14 13 12	11	10	9	8

Name	-	-	-	G8KRS2	G8KRS1	G8KRS0	G8K0S	G8KIS
Default	0	0	0	0	0	0	0	0
Bit #	7	6	5	4	3	2	1	0
Name	-	-	-	-	CLAD3	CLAD2	CLAD1	CLAD0
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: CLAD I/O Mode [3:0] (CLAD[3:0]). These bits control the CLAD clock I/O pins CLKA, CLKB, and CLKC. These register bits control which clock is used to recover the Rx clock from the line in the LIU. Table 1 shows more details.

Table 1. CLAD I/O Pin Decode Details

GL.CR2 CLAD[3:0]	CLKA PIN	CLKB PIN	CLKC PIN
00 XX	DS3 clock input	E3 clock input	STS-1 clock input
01 00	DS3 clock input	Low output	Low output
01 01	DS3 clock input	E3 clock output	Low output
01 10	DS3 clock input	Low output	STS-1 clock output
01 11	DS3 clock input	STS-1 clock output	E3 clock output
10 00	E3 clock input	Low output	Low output
10 01	E3 clock input	DS3 clock output	Low output
10 10	E3 clock input	Low output	STS-1 clock output
10 11	E3 clock input	STS-1 clock output	DS3 clock output
11 00	STS-1 clock input	Low output	Low output
11 01	STS-1 clock input	E3 output	Low output
11 10	STS-1 clock input	Low output	DS3 clock output
11 11	STS-1 clock input	DS3 clock output	E3 clock output

The CLAD supplies a reference clock to the receive LIUs. The receive LIU selects the clock frequency based on the mode selected by the user with the Framing Mode (FM) bits. The FM bits select the main framing operational modes. The CLAD output is also available as a transmit clock source if selected by the **PORT.CR3.CLADC** register bit.

Register Name: **PORT.CR3**
Register Description: **Port Control Register 3**
Register Address: **(0, 2, 4, 6) 44h**

Bit #	15	14	13	12	11	10	9	8
Name	-	-	RCLKS	RSOFOS	RPFPE	TCLKS	TSOFOS	TPFPE
Default	0	0	0	0	0	0	0	0
Bit #	7	6	5	4	3	2	1	0
Name	P8KRS1	P8KRS0	P8KREF	LOOPT	**CLADC**	RFTS	TFTS	TLTS
Default	0	0	0	0	**0**	0	0	0

Bit 3: CLAD Transmit Clock Source Control (CLADC). This bit is used to enable the CLAD clocks as

the source of the internal transmit clock. This bit's function is conditional on other control bits.

0 = Use CLAD clocks for the transmit clock as appropriate.
1 = Do not use CLAD clocks for the transmit clock. (If no loopback is enabled, TCLKIn is the source.)

Conclusion

The DS325X, DS316X, DS317X, and DS318X devices contain a CLAD function, which can be very useful to create multiple clocks for LIU reference clocks or to function as transmit clocks for the user's application. For further questions about the CLAD operation on Maxim parts, please contact the Maxim Telecommunications applications support team by email at telecom.support@maximintegrated.com or, in the USA, call 972-371-6555.

Related Parts		
DS3161	Single/Dual/Triple/Quad ATM/Packet PHYs for DS3/E3/STS-1	
DS3162	Single/Dual/Triple/Quad ATM/Packet PHYs for DS3/E3/STS-1	
DS3163	Single/Dual/Triple/Quad ATM/Packet PHYs for DS3/E3/STS-1	
DS3164	Single/Dual/Triple/Quad ATM/Packet PHYs for DS3/E3/STS-1	
DS3171	Single/Dual/Triple/Quad DS3/E3 Single-Chip Transceivers	Free Samples
DS3172	Single/Dual/Triple/Quad DS3/E3 Single-Chip Transceivers	Free Samples
DS3173	Single/Dual/Triple/Quad DS3/E3 Single-Chip Transceivers	
DS3174	Single/Dual/Triple/Quad DS3/E3 Single-Chip Transceivers	Free Samples
DS3181	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples
DS3182	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples
DS3183	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	
DS3184	Single/Dual/Triple/Quad ATM/Packet PHYs with Built-In LIU	Free Samples
DS3251	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3252	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3253	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples
DS3254	Single/Dual/Triple/Quad DS3/E3/STS-1 LIUs	Free Samples

More Information

For Technical Support: http://www.maximintegrated.com/support
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Application Note 3609: http://www.maximintegrated.com/an3609
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