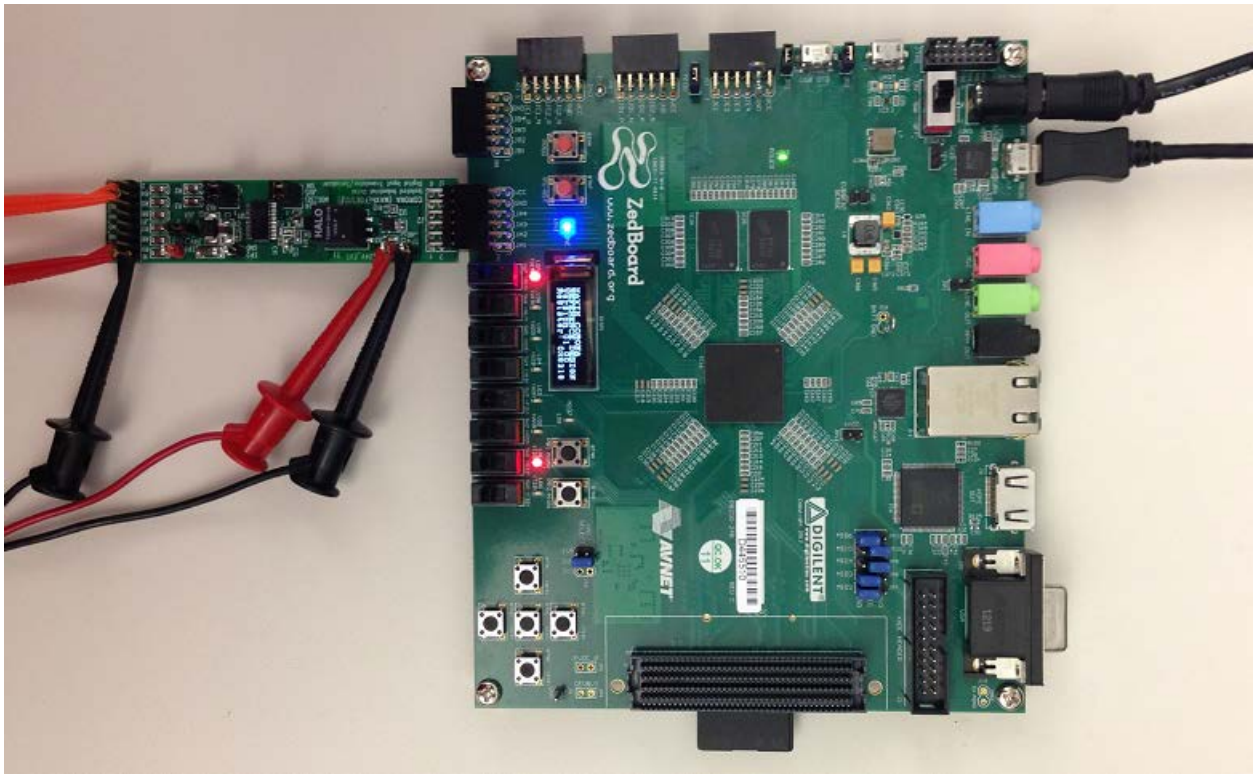
Corona (MAXREFDES12#) ZedBoard Quick Start Guide

Rev 0; 4/13



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1. Required Equipment

- PC with Windows® OS with Xilinx® ISE®/SDK version 14.2 or later and one USB port (Refer to Xilinx AR# 51895 if you installed ISE WebPACK™ design software on your PC.)
- License for Xilinx EDK/SDK version 14.2 or later (free WebPACK license is OK)
- Corona (MAXREFDES12#) board
- ZedBoard™ development kit
- One 24V 1A DC power supply

2. Overview

Below is a high-level overview of the steps required to quickly get the Corona design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. **The Corona (MAXREFDES12#) subsystem reference design will be referred to as Corona throughout this document.**

1) Connect the Corona board to the JA1 port of a ZedBoard as shown in Figure 1. Ensure the connector is aligned as shown in Figure 2.
2) Download the latest **RD12V01_00.ZIP** file located at the Corona page.
3) Extract the **RD12V01_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Use Xilinx SDK to download and run the executable file (.ELF) on one of the two ARM® Cortex™ -A9 processors.

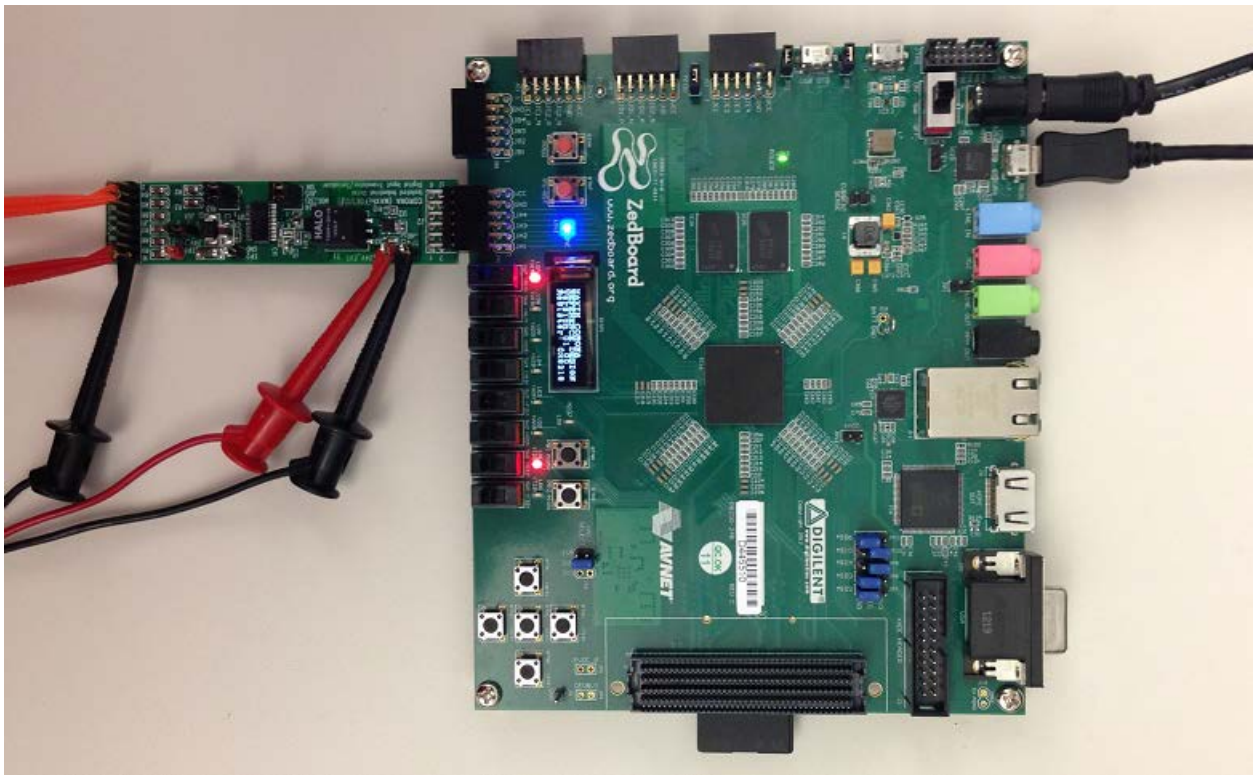


Figure 1. Corona Board Connected to ZedBoard Kit

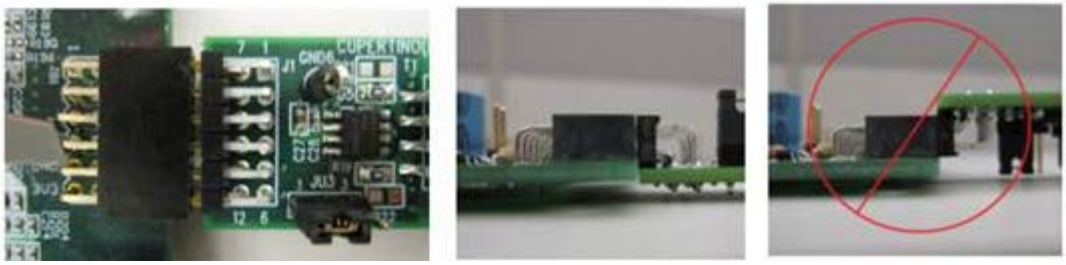


Figure 2. Pmod™ Connector Alignment

3. Included Files

The top level of the hardware design is a Xilinx ISE Project Navigator Project (.XISE) for Xilinx ISE version 14.2. The Verilog-based top.v module provides FPGA/board net connectivity, allows HDL interaction with peripherals, and instantiates the wrapper that carries both the Zynq Processing System and (I^2C, SPI, GPIO, UART) soft peripherals that interface to the Pmod ports. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Corona subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

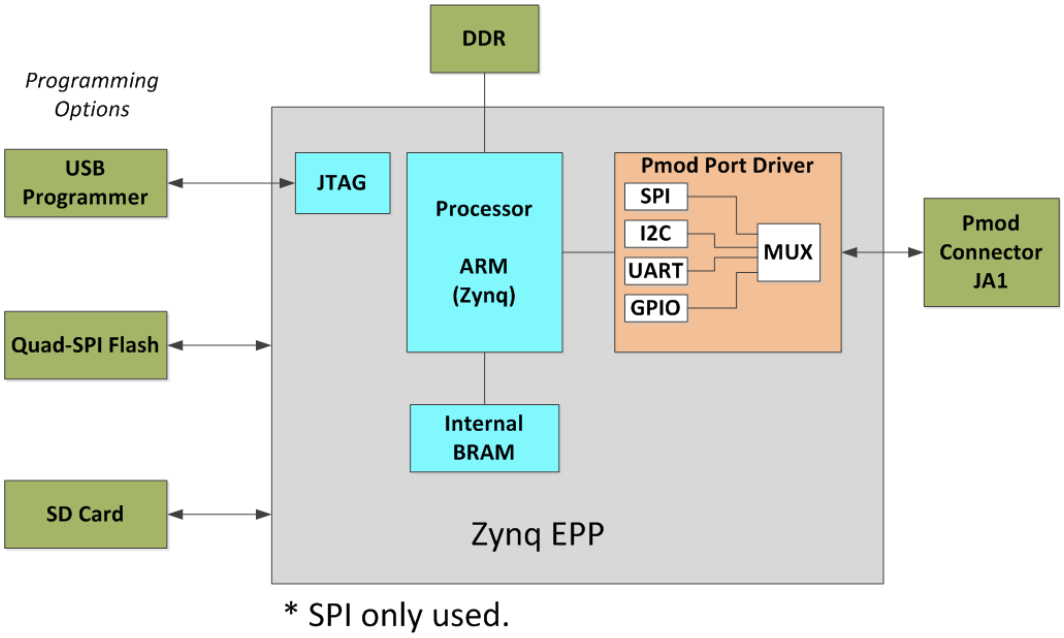


Figure 3. Block Diagram of FPGA Hardware Design

4. Procedure

1. Connect the Corona board to the JA1 port of a ZedBoard as shown in Figure 1.

2. Connect the 24V DC power supply positive terminal to the TP3 connector on the Corona board. Connect the 24V DC power supply ground terminal to the TP4 connector on the Corona board.

3. Power up the ZedBoard by sliding the SW8 switch on the ZedBoard to the ON position.

4. Download the latest **RD12V01_00.ZIP** file at **www.maximintegrated.com/AN5611**. All files available for download are available at the bottom of the page.

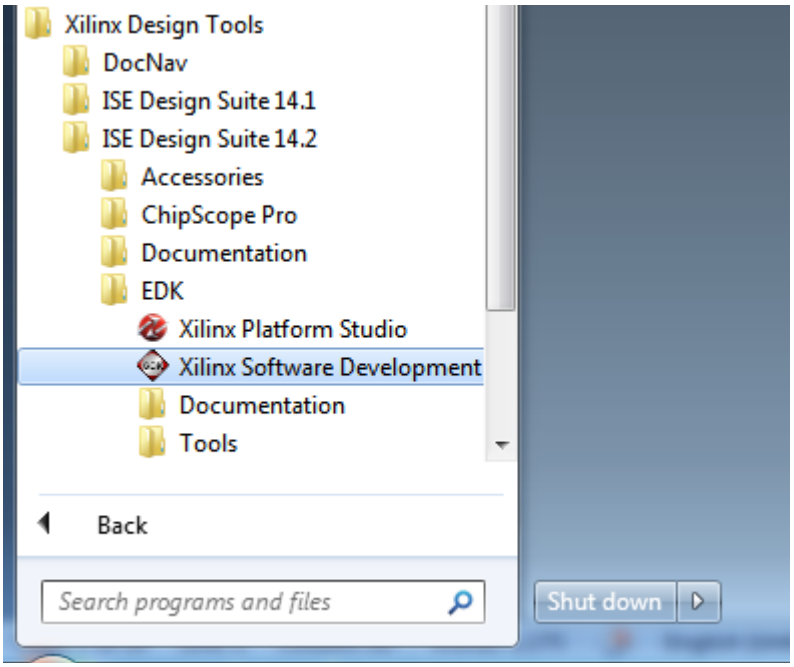
5. Extract the **RD12V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the maximum path length limitation in Windows (260 characters) should not be exceeded.

   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD12V01_00.ZIP
   (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD12V01_00**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

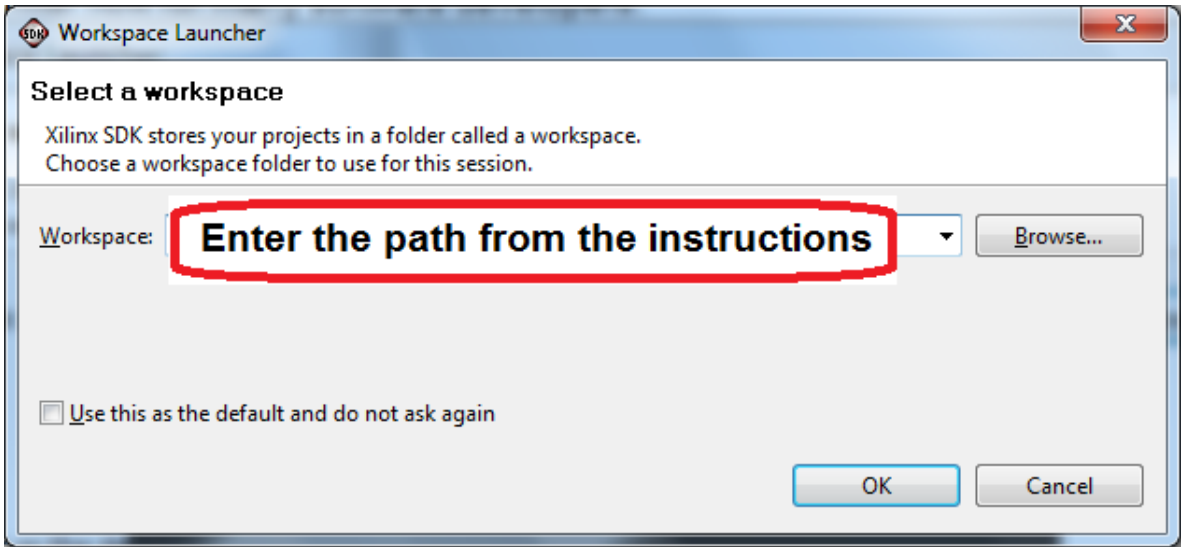
6. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



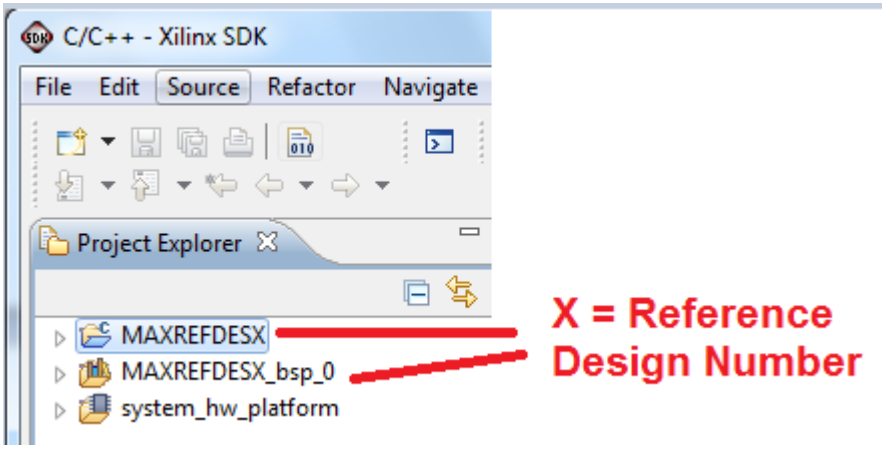
7. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

C:\designs\maxim\RD12V01_00\RD12_ZED_V01_00\Design_Files\sdkWorkspace

Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



8. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

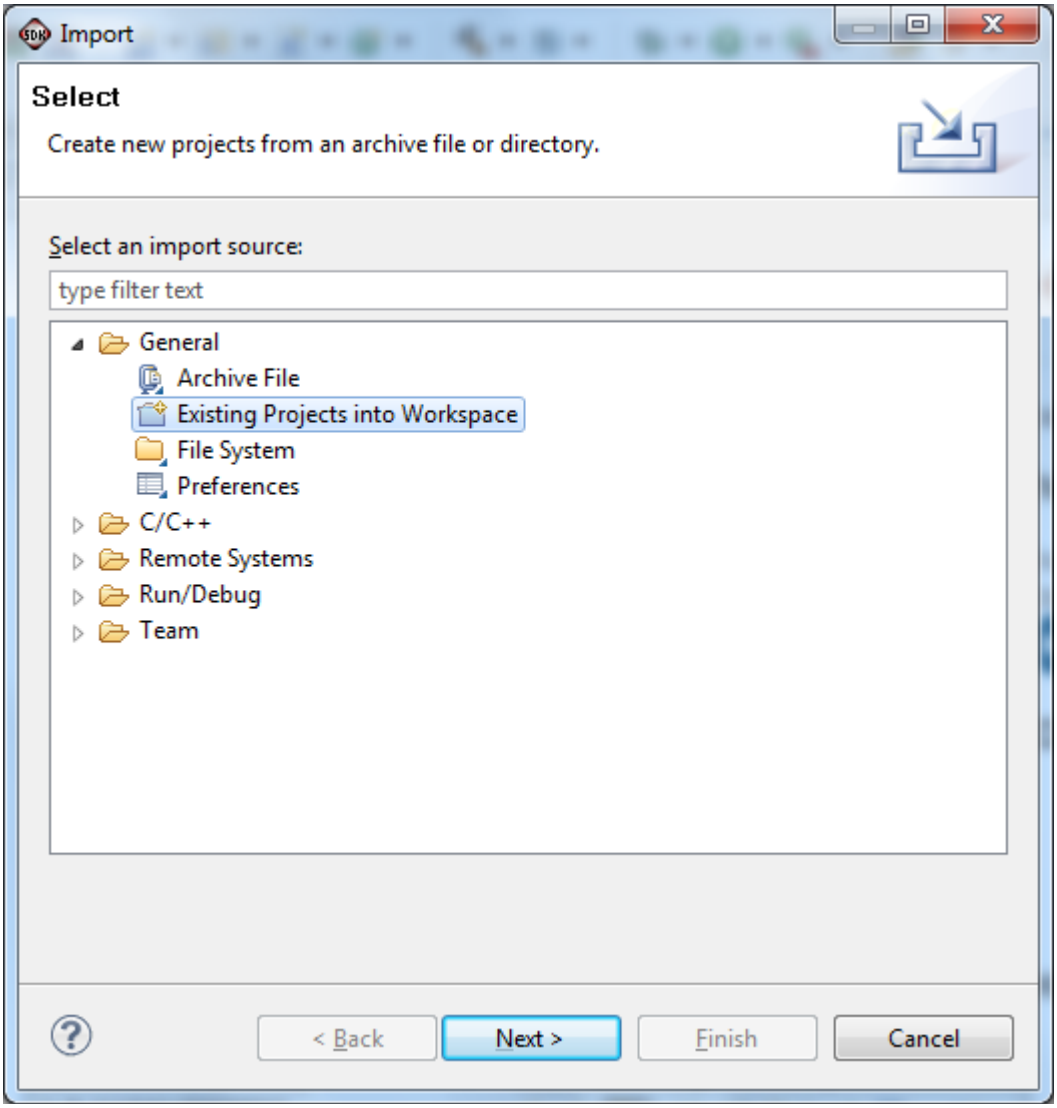


9. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

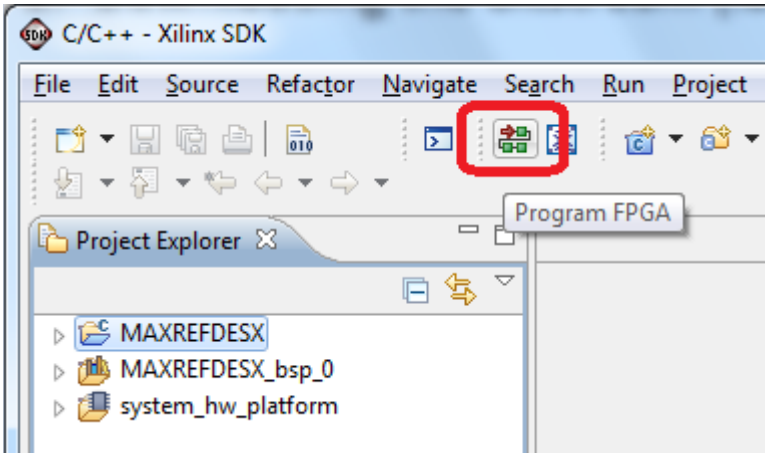
   C:\designs\maxim\RD12V01_00\RD12_ZED_V01_00\Design_Files\sdkWorkspace

   and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

   Click **Finish** to import the projects.



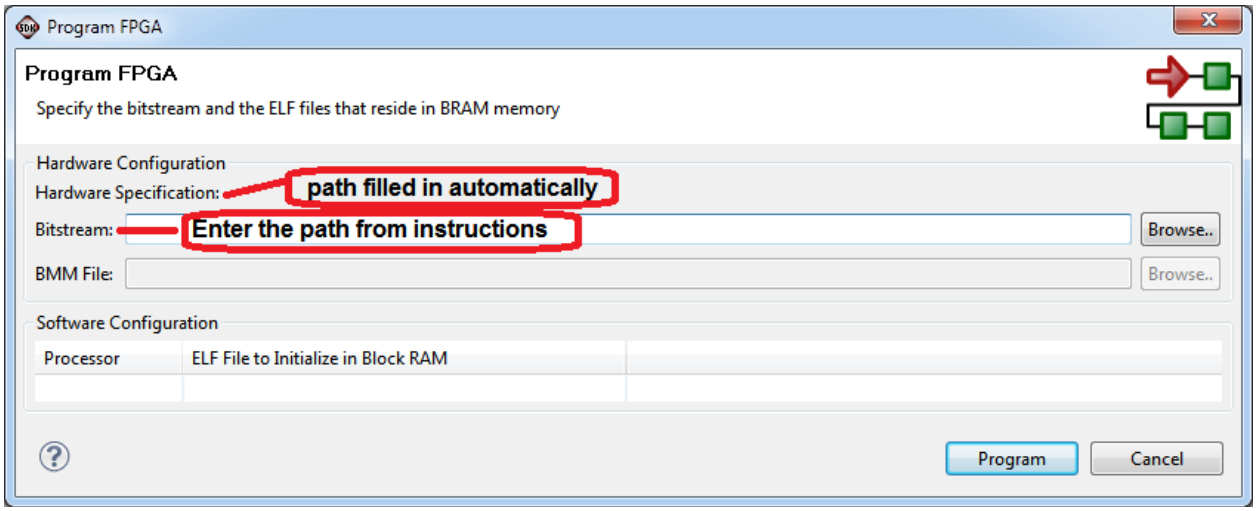
10. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).



The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected. Be sure to select the .BIT file by using the paths below.

Bitstream:
C:\designs\maxim\RD12V01_00\RD12_ZED_V01_00\Design_Files\top.bit

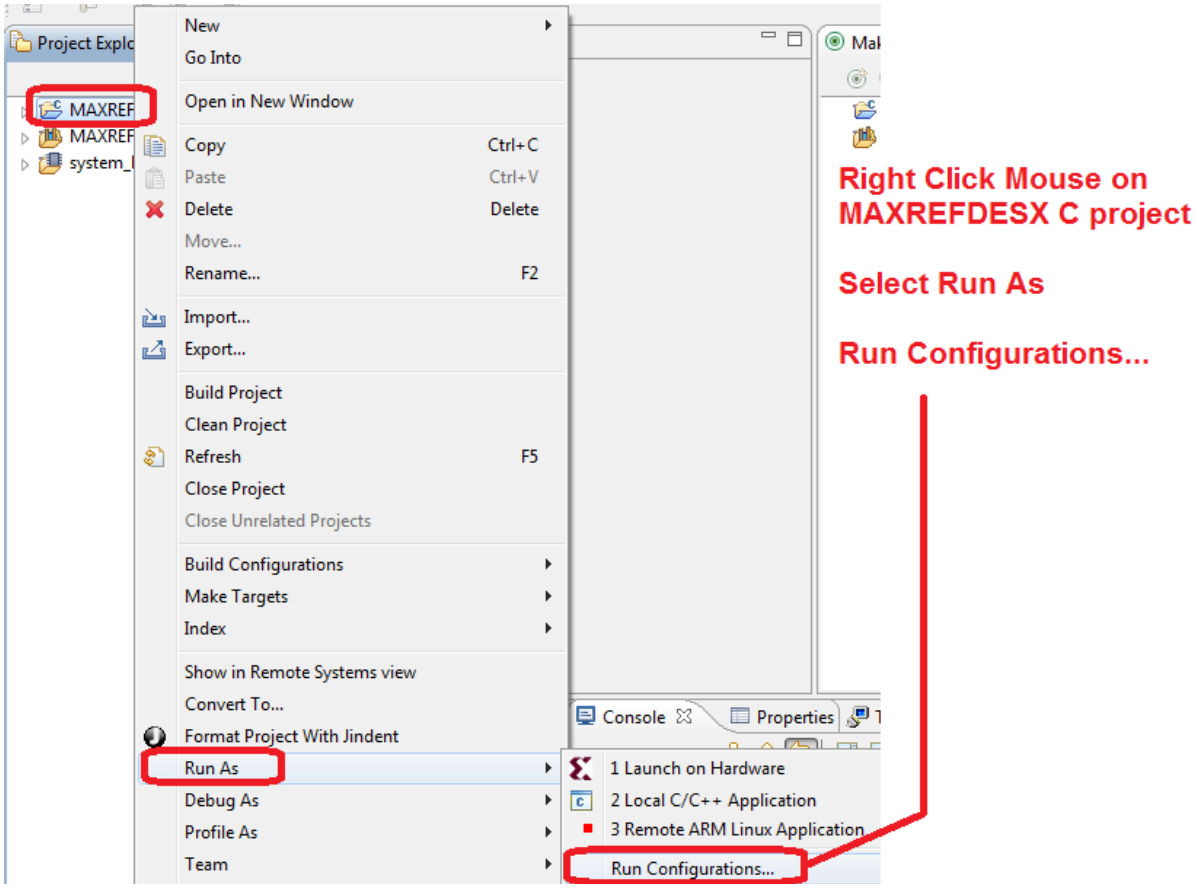
Press **Program**.



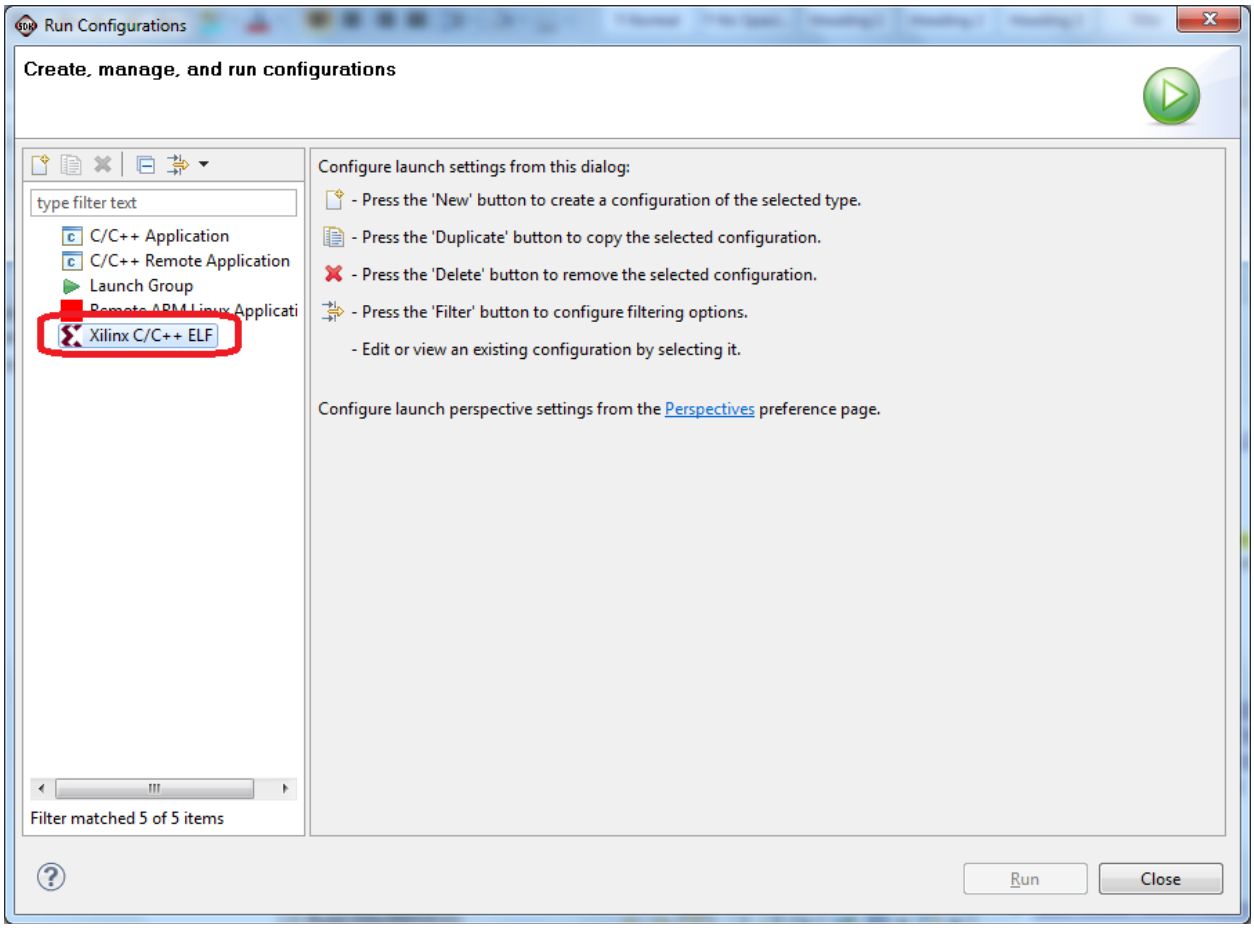
It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

11. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the ARM Cortex-A9 processor using the following steps.

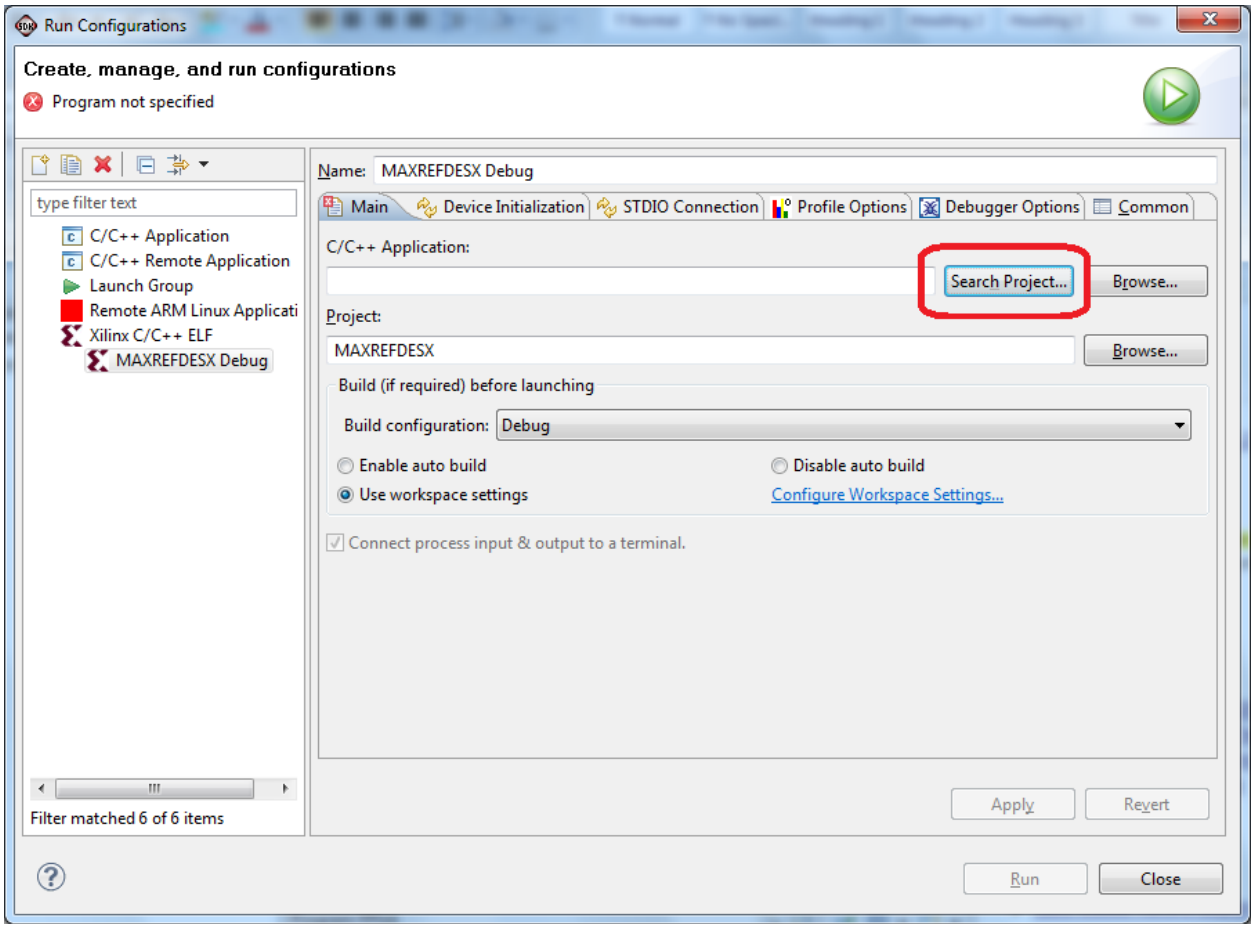
    Right-click the mouse while the **MAXREFDES12 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



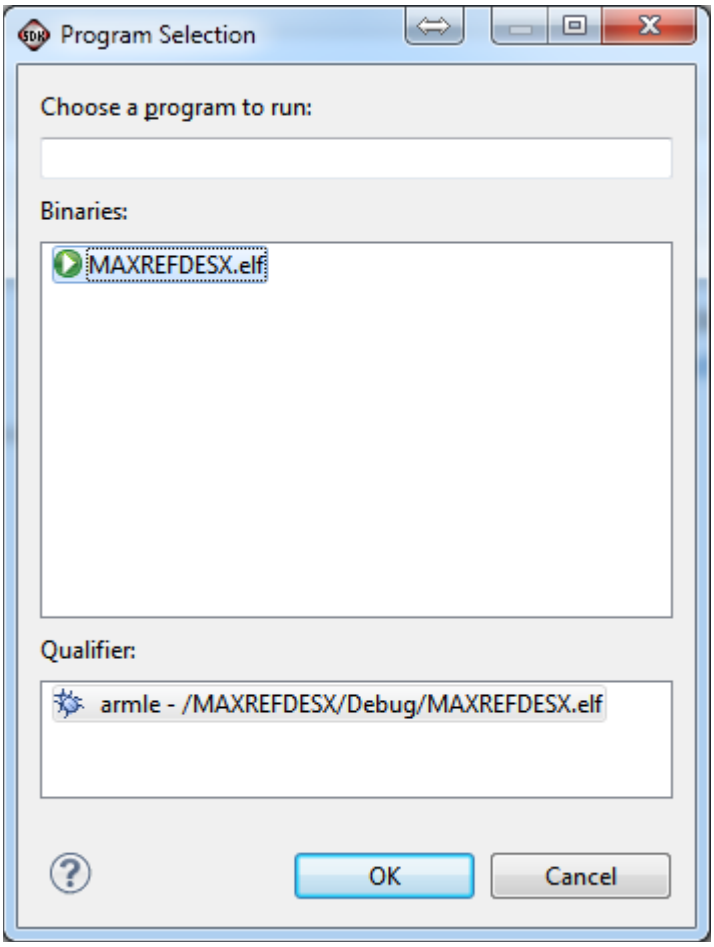
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



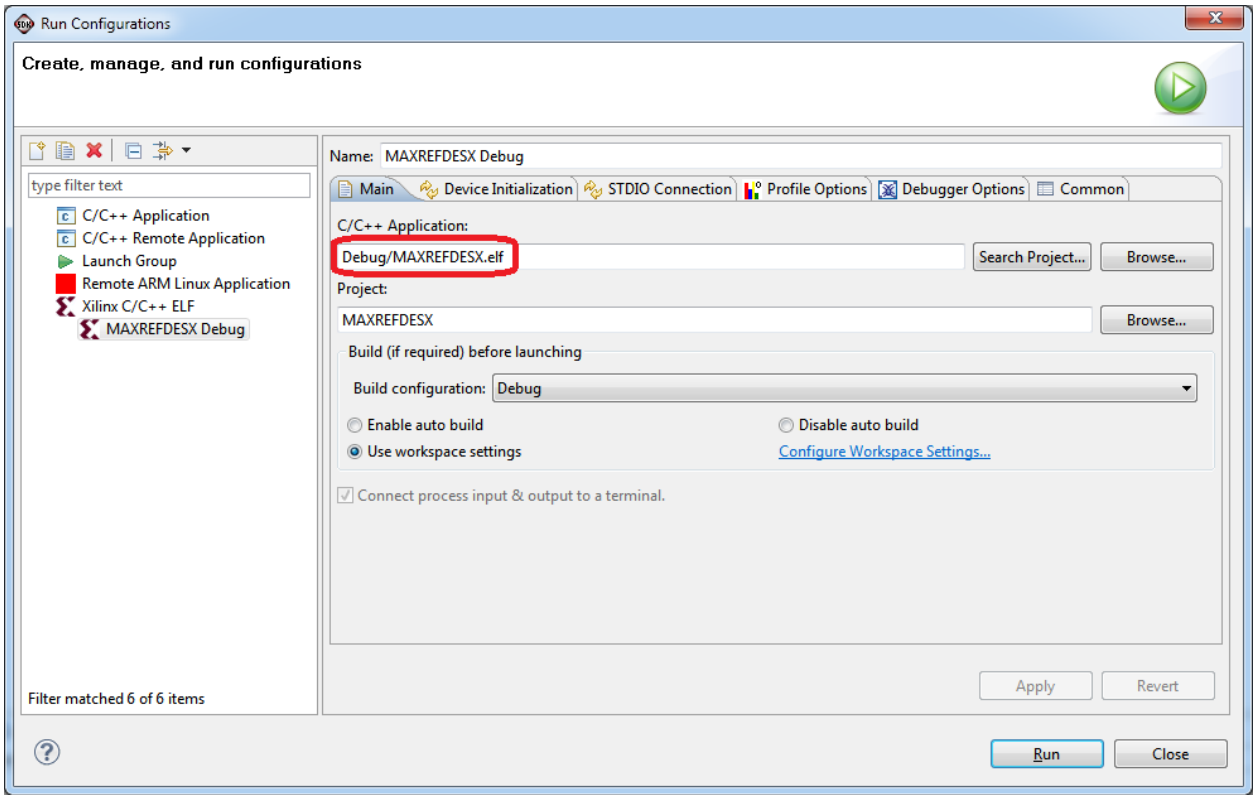
Next, press the **Search Project** button.



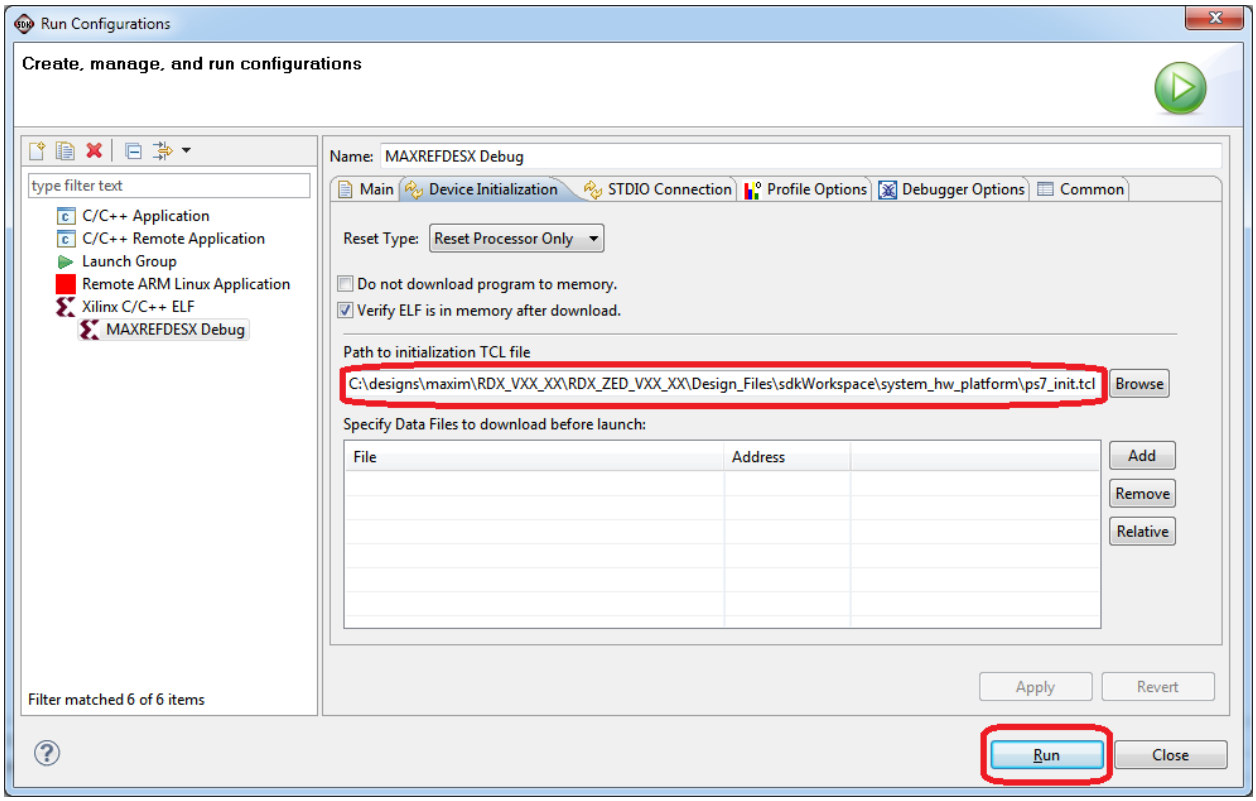
Double-click on the **MAXREFDES12.elf** binary.



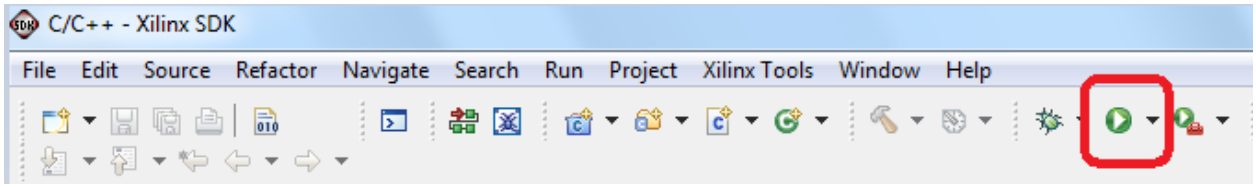
Verify the application is selected on the **Main** tab.



On the **Device Initialization** tab, click the **Browse…** button to select the correct initialization TCL file, then press the **Run** button.



Once the Debug/MAXREFDES12 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

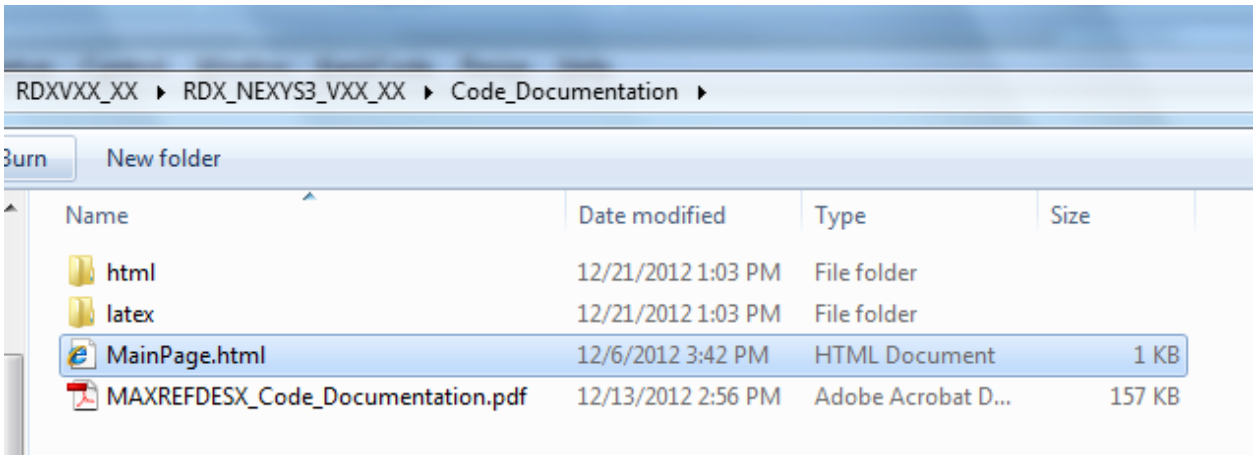


At this point, the application is running on the ARM Cortex-A9 processor. The LEDs LD7–LD0 on the ZedBoard indicate the voltage levels of the digital input channels IN8–IN0, respectively. LED ON indicates a high-voltage input, LED OFF indicates a low-voltage input. At the same time, the OLED panel on the ZedBoard displays the MAX31911 16-bit register value in HEX format.

Change the digital input voltages to verify the register value follows the changes properly.

5. Code Documentation

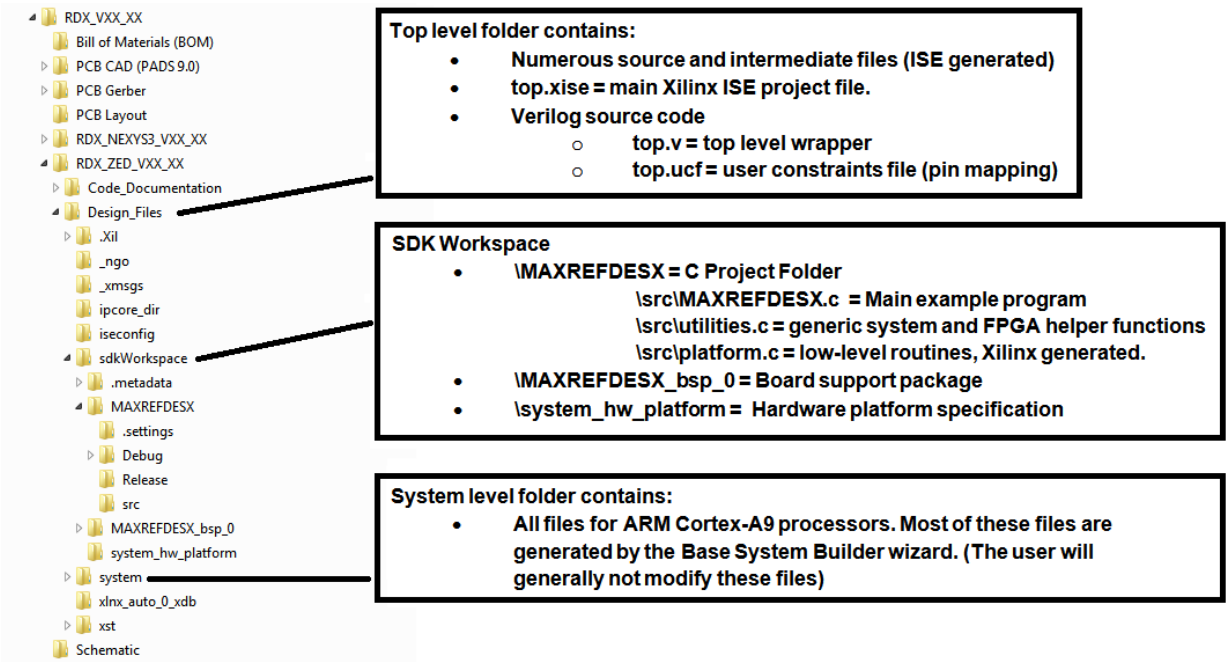
Code documentation can be found at:
C:\...\RD12V01_00\RD12_ZED_V01_00\Code_Documentation



To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES12_Code_Documentation.pdf** file.

6. Appendix A: Project Structure and Key Filenames



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Xilinx is a registered trademark and registered service mark of Xilinx, Inc.
ZedBoard is a trademark of Avnet, Inc.

8. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/13	Initial release	–